

54/74259—See 9334
54LS/74LS259 (Preliminary data)

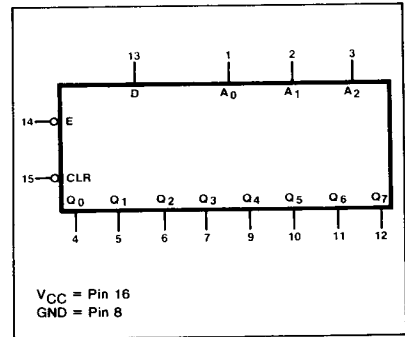
DESCRIPTION

The "259" is an 8-Bit Addressable Latch with these control inputs; three Address inputs (A₀, A₁, A₂), an active LOW Enable input (\bar{E}) and an active LOW Clear input (CLR). Each latch has a common D input and a separate Q output. The "259" combines the features of a 1-of-8 demultiplexer and 8-bit transparent latch into one 16 pin package.

FEATURES

- Combines demultiplexer and 8-bit latch
- Serial-to-Parallel capability
- Output from each storage bit available
- Random (Addressable) data entry
- Easily expandable
- Common Clear input
- Useful as dual 1-of-8 active HIGH decoder
- See the NE590 for 250 mA output version

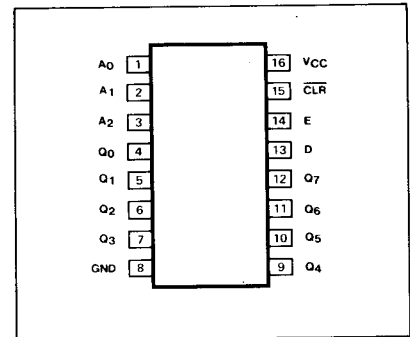
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C	MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74LS259N	
Ceramic DIP	N74LS259F	S54LS259F
Flatpak		S54LS259W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION	54/74	54S/74S	54LS/74LS
A ₀ , A ₁ , A ₂	Address inputs			I _H (μA) I _L (mA) 20 -0.4
D	Data input			I _H (μA) I _L (mA) 20 -0.4
\bar{E}	Latch Enable (active LOW) input			I _H (μA) I _L (mA) 40 -0.8
CLR	Clear (active LOW) input			I _H (μA) I _L (mA) 20 -0.4
Q ₀ -Q ₇	Latch outputs			I _{OH} (μA) I _{OL} (mA) -400 4/8 (a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "259" Addressable Latch has four distinct modes of operation and are selectable by controlling the Clear and Enable inputs (see the function table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, (CLR = \bar{E} = LOW) addressed outputs will follow the level of the D inputs with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the address and data inputs.

MODE SELECT—FUNCTION TABLE

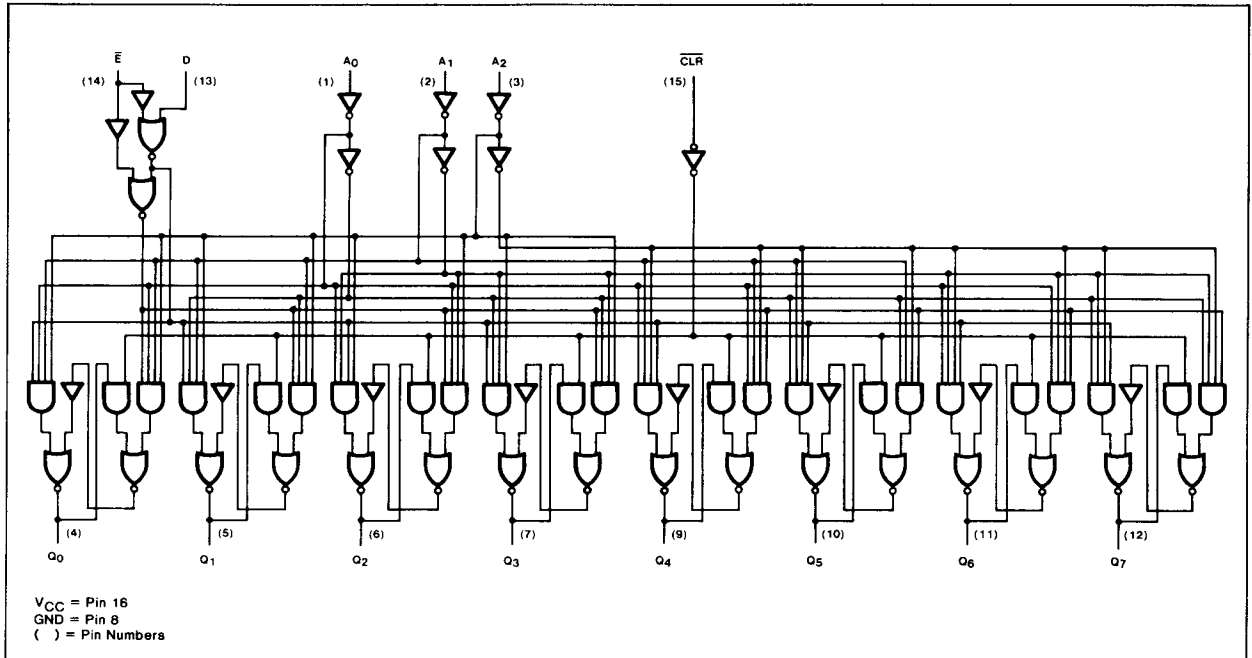
OPERATING MODE	INPUTS						OUTPUTS							
	CLR	\bar{E}	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
Clear	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (active HIGH decoder when D=H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L

	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
Store (do nothing)	H	H	X	X	X	X	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
Addressable latch	H	L	d	L	L	L	Q=d	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	H	L	L	q ₀	Q=d	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	H	L	q ₀	q ₁	Q=d	q ₃	q ₄	q ₅	q ₆	q ₇

	H	L	d	H	H	H	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	Q=d

H = HIGH voltage level steady state
 L = LOW voltage level steady state
 X = Don't care
 d = HIGH or LOW data one setup time prior to LOW-to-HIGH Enable transition
 q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max						36	mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
						C _L = 15pF R _L = 2kΩ		
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay t _{PHL} Enable to output	Figure 1						35 24	ns ns
t _{PLH} Propagation delay t _{PHL} Data to output	Figure 2						32 21	ns ns
t _{PLH} Propagation delay t _{PHL} Address to output	Figure 3						38 29	ns ns
t _{PHL} Propagation delay clear to output	Figure 4						27	ns

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _w Enable pulse width	Figure 1					15		ns
t _w Clear pulse width	Figure 4					15		ns
t _s (H) Setup time HIGH Data to Enable	Figure 5					20		ns
t _h (H) Hold time HIGH Data to Enable	Figure 5					0		ns
t _s (L) Setup time LOW Data to Enable	Figure 5					15		ns
t _h (L) Hold time LOW Data to Enable	Figure 5					0		ns
t _s Setup time Address to Enable ^(c)	Figure 6					0		ns
t _h Hold time Address to Enable ^(d)	Figure 6					10		ns

NOTES

- c. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
- d. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

AC WAVEFORMS

