National Semiconductor

DM54S200/DM74S200 256-Bit (256 × 1) TRI-STATE® RAM

general description

The DM54S200/DM74S200 256-bit active-element memories are monolithic transistor-transistor logic (TTL) integrated circuits organized as 256 words of one bit each. They are fully decoded and have three gated memory-enable inputs to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors which reduce the low-level input current requirement to a maximum of −0.25 milliamperes, only one-eighth that of a normalized Series 54S/74S load factor. The memory-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast-rise-time characteristics of the TTL totem-pole output.

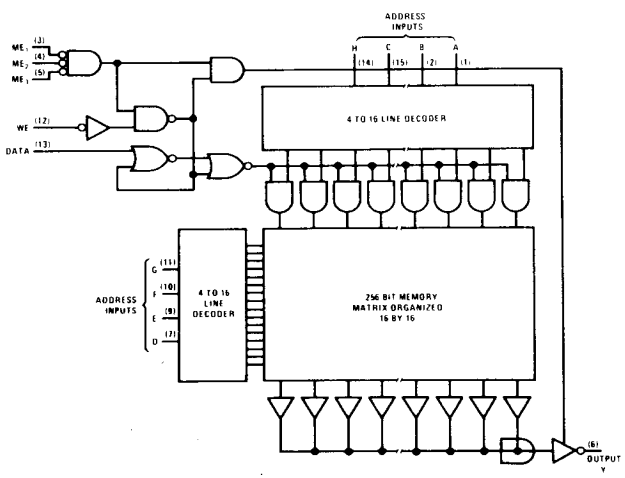
Write Cycle: The complement of the information at the data input is written into the selected location when all memory-enable inputs and write-enable input are low. While the write-enable input is low, the output is in the high-impedance state. When a number of outputs are bus-connected, this high-impedance output state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

Read Cycle: The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the three memory-enable inputs are low. When any one of the memory enable inputs is high, the output will be in the high-impedance state.

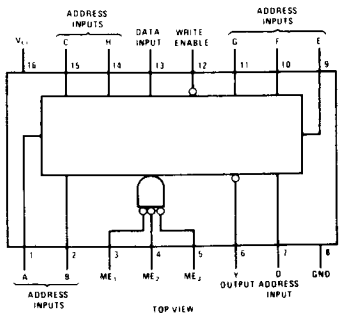
features

- Schottky-clamped for high-speed memory systems:
  - Access from memory-enable inputs 20 ns typ
  - Access from address inputs 31 ns typ
  - Power dissipation 1.7 mW/bit typ
- TRI-STATE output for driving bus-organized systems and/or highly capacitive loads
- Fully decoded, organized as 256 words of one bit each
- Compatible with most TTL and DTL logic circuits
- Multiple memory-enable inputs to minimize external decoding

block and connection diagrams



Dual-In-Line Package



Order Number DM54S200J or DM74S200J
See NS Package J16A

Order Number DM74S200N
See NS Package N16A

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S200	4.5	5.5	V
DM74S200	4.75	5.25	V
Temperature (T_A)			
DM54S200	−55	+125	°C
DM74S200	0	+70	°C

recommended operating conditions

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Output Current (I_{OH})					
DM54S200				−2.0	mA
DM74S200				−5.2	mA
Low Level Output Current (I_{OL})				16	mA
Width of Write Enable Pulse (t_W)					
DM54S200		50			ns
DM74S200		40			ns
Setup Time (t_{SETUP})					
Address to Write Enable		0			ns
Data to Write Enable		0			ns
Memory Enable to Write Enable		0			ns
Hold Time (t_{HOLD})					
Address from Write Enable		10			ns
Data from Write Enable		10			ns
Memory Enable from Write Enable		0			ns

electrical characteristics (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
High Level Input Voltage (V_{IH})			2.0			V
Low Level Input Voltage (V_{IL})					0.8	V
Input Clamp Voltage (V_I)	V_{CC} = Min, I_I = −18 mA				−1.2	V
High Level Output Voltage (V_{OH})	V_{CC} = Min, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OH} = Max		2.4			V
Low Level Output Voltage (V_{OL})	V_{CC} = Min, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OL} = Max	DM54S200			0.5	V
		DM74S200			0.45	
Off State (High Impedance State) Output Current ($I_{O(OFF)}$)	V_{CC} = Max, V_{IH} = 2.0V					
	V_O = 2.4V				50	μA
	V_O = 0.5V				−50	μA
Input Current at Maximum Input Voltage (I_I)	V_{CC} = Max, V_I = 5.5V				1.0	mA
High Level Input Current (I_{IH})	V_{CC} = Max, V_I = 2.7V				25	μA
Low Level Input Current (I_{IL})	V_{CC} = Max, V_I = 0.5V				−250	μA
Short Circuit Output Current (I_{OS}) (Note 3)	V_{CC} = Max		−30		−100	mA
Supply Current (I_{CC})	V_{CC} = Max (Note 5)			87	130	mA

switching characteristics All Typical Values are at V_{CC} = 5.0V, T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	PARAMETER CONDITIONS	TEST CONDITIONS	DM54S200			DM74S200			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Access Time from Address			33	70		33	50	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output	Access Time from Address			29	70		29	50	ns
t_{ZH}	Output Enable Time to High Level	Access Times from Memory Enable	C_L = 30 pF, R_L = 300Ω		21	45		21	35	ns
t_{ZL}	Output Enable Time to Low Level	Access Times from Memory Enable			10	30		10	20	ns
t_{ZH}	Output Enable Time to High Level	Sense Recovery Times from Write Enable			24	50		24	40	ns
t_{ZL}	Output Enable Time to Low Level	Sense Recovery Times from Write Enable			12	50		12	40	ns
t_{HZ}	Output Disable Time from High Level	Disable Times from Memory Enable			7.0	30		7.0	20	ns
t_{LZ}	Output Disable Time from Low Level	Disable Times from Memory Enable	C_L = 5.0 pF R_L = 300Ω		20	45		20	35	ns
t_{HZ}	Output Disable Time from High Level	Disable Times from Write Enable			13	40		13	30	ns
t_{LZ}	Output Disable Time from Low Level	Disable Times from Write Enable			16	40		16	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for DM54S200 and across the 0°C to +70°C range for the DM74S200. All typicals are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: Duration of the short-circuit should not exceed one second.

Note 4: All voltage values are with respect to network ground terminal.

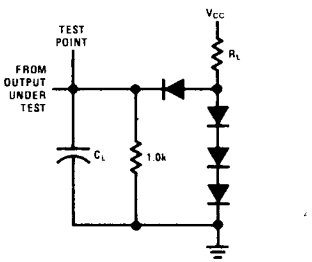
Note 5: I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.

truth table

FUNCTION	INPUTS		OUTPUT
	MEMORY ENABLE†	WRITE ENABLE	
Write (Store Complement of Data)	L	L	High Impedance
Read	L	H	Stored Data
Inhibit	H	X	High Impedance

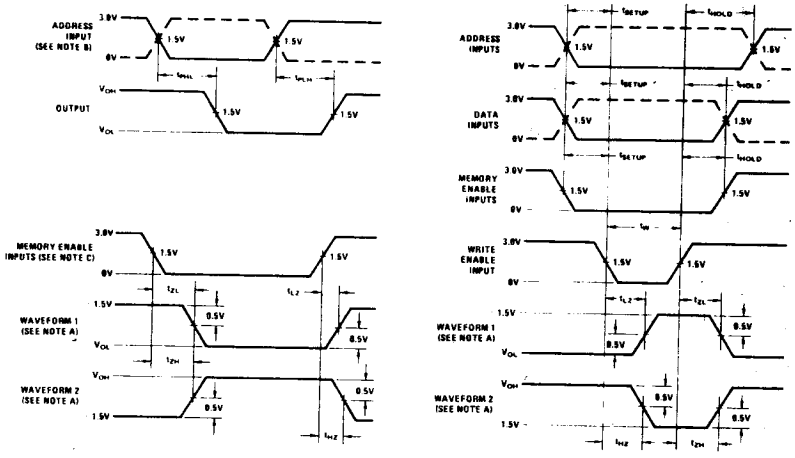
H = high level, L = low level, X = irrelevant
†For memory enable: L = all ME inputs low; H = one or more ME inputs high

ac test circuit



C_L INCLUDES PROBE AND JIG CAPACITANCE.
ALL DIODES ARE 1N3064.

switching time waveforms



NOTE A: WAVEFORM 1 IS FOR THE OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW EXCEPT WHEN DISABLED. WAVEFORM 2 IS FOR THE OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH EXCEPT WHEN DISABLED.

NOTE B: WHEN MEASURING DELAY TIMES FROM ADDRESS INPUTS, THE MEMORY ENABLE INPUTS ARE LOW AND THE WRITE ENABLE INPUT IS HIGH.

NOTE C: WHEN MEASURING DELAY TIMES FROM MEMORY ENABLE INPUTS, THE ADDRESS INPUTS ARE STEADY STATE AND THE WRITE ENABLE INPUT IS HIGH.

NOTE D: INPUT WAVEFORMS ARE SUPPLIED BY PULSE GENERATORS HAVING THE FOLLOWING CHARACTERISTICS: $t_r = t_f = 2.5$ ns, $t_w = 25$ ns, PRR = 1.8 MHz, AND $Z_{OUT} \approx 50\Omega$.