

Document No.	853-0148
ECN No.	86487
Date of Issue	November 11, 1986
Status	Product Specification
Memory Products	

# 82S126 82S129

## 1K-bit TTL bipolar PROM

### DESCRIPTION

The 82S126 and 82S129 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S126 and 82S129 devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 2 Chip Enable inputs for ease of memory expansion. They feature either Open Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S126 and 82S129 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information, consult the Signetics Military Data Handbook.

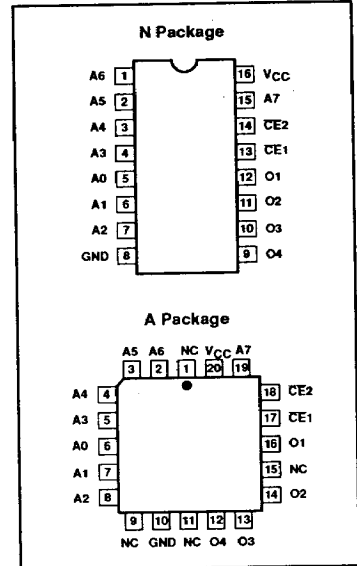
### FEATURES

- Address access time: 50ns max
- Power dissipation: 0.5mW/bit typ
- Input loading:  $-100\mu\text{A}$  max
- On-chip address decoding
- Two Chip Enable inputs
- Output options:
  - N82S126: Open Collector
  - N82S129: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

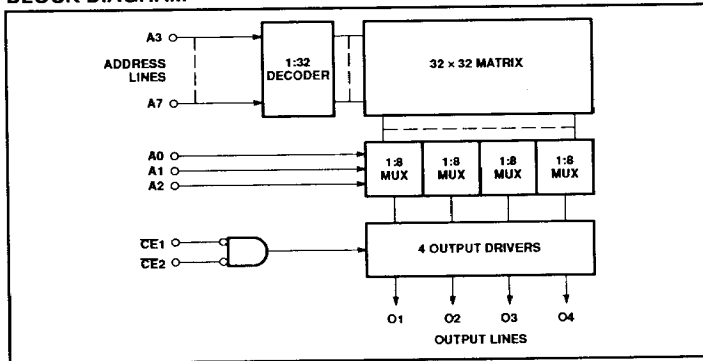
### APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Format conversion
- Hardwired algorithms
- Random logic
- Code conversion

### PIN CONFIGURATIONS



### BLOCK DIAGRAM



## 1K-bit TTL bipolar PROM (256 × 4)

82S126 / 82S129

## ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Plastic Dual-In-Line 300mil-wide	N82S126 N, N82S129 N
20-Pin Plastic Leaded Chip Carrier 350mil-square	N82S126 A, N82S129 A

## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	+7.0	V <sub>DC</sub>
V <sub>IN</sub>	Input voltage	+5.5	V <sub>DC</sub>
V <sub>OH</sub>	Output voltage High (82S126)	+5.5	V <sub>DC</sub>
V <sub>O</sub>	Output voltage Off-State (82S129)	+5.5	V <sub>DC</sub>
T <sub>amb</sub>	Operating temperature range	0 to +75	°C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

## DC ELECTRICAL CHARACTERISTICS

0°C ≤ T<sub>amb</sub> ≤ +75°C, 4.75V ≤ V<sub>CC</sub> ≤ 5.25V

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1,2</sup>	LIMITS			UNIT
			MIN	TYP <sup>3</sup>	MAX	
<b>Input voltage</b>						
V <sub>IL</sub>	Low	I <sub>IN</sub> = -12mA	2.0		0.8	V
V <sub>IH</sub>	High					
V <sub>IC</sub>	Clamp				-1.2	V
<b>Output voltage</b>						
V <sub>OL</sub>	Low	CE1,2 = Low I <sub>OUT</sub> = 16mA	2.4		0.45	V
V <sub>OH</sub>	High (82S129)	I <sub>OUT</sub> = -2.0mA				V
<b>Input current</b>						
I <sub>IL</sub>	Low	V <sub>IN</sub> = 0.45V			-100	μA
I <sub>IH</sub>	High	V <sub>IN</sub> = 5.5V			40	μA
<b>Output current</b>						
I <sub>OLK</sub>	Leakage (82S126)	CE1 or CE2 = High, V <sub>OUT</sub> = 5.5V			40	μA
I <sub>OZ</sub>	Hi-Z state (82S129)	CE1 or CE2 = High, V <sub>OUT</sub> = 5.5V			40	μA
		CE1 or CE2 = High, V <sub>OUT</sub> = 0.5V			-40	μA
I <sub>OS</sub>	Short circuit (82S129) <sup>4</sup>	CE1,2 = Low, V <sub>OUT</sub> = 0V, High stored	-15		-70	mA
<b>Supply current<sup>5</sup></b>						
I <sub>CC</sub>		V <sub>CC</sub> = 5.25V			120	mA
<b>Capacitance</b>						
C <sub>IN</sub>	Input	CE1 or CE2 = High, V <sub>CC</sub> = 5.0V V <sub>IN</sub> = 2.0V			5	pF
C <sub>OUT</sub>	Output	V <sub>OUT</sub> = 2.0V			8	pF

## NOTES:

- Positive current is defined as into the terminal referenced.
- All voltages with respect to network ground.
- Typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = +25°C.
- Duration of short circuit should not exceed 1 second.
- Measured with all inputs grounded and all outputs open.

# 1K-bit TTL bipolar PROM (256 × 4)

82S126 / 82S129

## AC ELECTRICAL CHARACTERISTICS

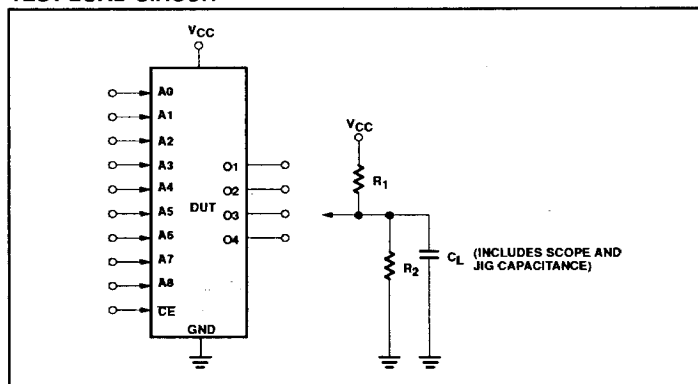
$R_1 = 270\Omega$ ,  $R_2 = 600\Omega$ ,  $C_L = 30\text{pF}$ ,  $0^\circ\text{C} \leq T_{\text{amb}} \leq +75^\circ\text{C}$ ,  $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				MIN	TYP <sup>1</sup>	MAX	
<b>Access time<sup>2</sup></b>							
$t_{AA}$		Output	Address		40	50	ns
$t_{CE}$		Output	Chip Enable			25	ns
<b>Disable time<sup>3</sup></b>							
$t_{CD}$		Output	Chip Disable			25	ns

**NOTES:**

1. Typical values are at  $V_{\text{CC}} = 5\text{V}$ ,  $T_{\text{amb}} = +25^\circ\text{C}$ .
2. Tested at an address cycle time of  $1\mu\text{s}$ .
3. Measured at a delta of  $0.5\text{V}$  from Logic Level with  $R_1 = 750\Omega$ ,  $R_2 = 750\Omega$ ,  $C_L = 5\text{pF}$ .

### TEST LOAD CIRCUIT



### VOLTAGE WAVEFORMS

