Philips Components–Signetics

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Status	Product Specification
Memory Products	

82LS16
256-bit TTL bipolar RAM

DESCRIPTION

The 82LS16 is a Read/Write memory array which features 3-State outputs for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 Chip Enable inputs and PNP input transistors which reduce input loading.

During Write operation, the logical state of the output follows the complement of the data input being written. This feature allows faster execution of Write/Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following Write cycle.

The 82LS16 has fast Read access and Write cycle times, as well as low power requirements and thus is ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, where power limitations are of major concern.

Ordering codes are listed in the Ordering Information Table

APPLICATIONS

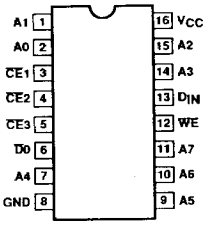
- Buffer memory
- Writable control store
- Memory mapping
- Push down stack
- Scratch pad

FEATURES

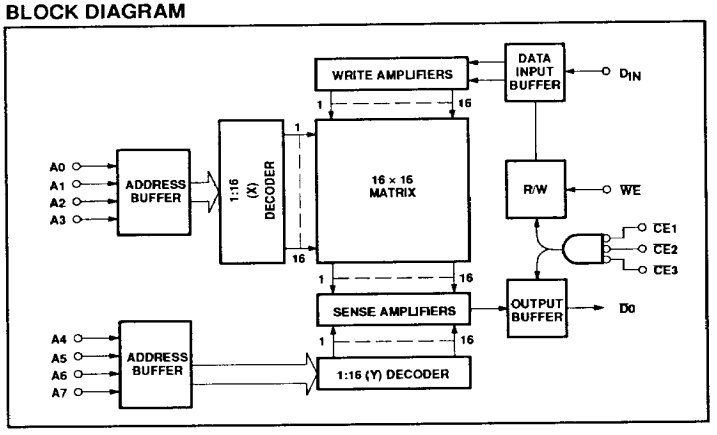
- Address access time: 40ns max
- Write cycle time: 45ns max
- Power dissipation: 0.98mW/bit typ
- Input loading: -100μA max
- Output follows complement of data input during Write
- On-chip address decoding
- Three Chip Enable inputs
- Output: 3-State
- Schottky clamped
- TTL compatible

PIN CONFIGURATION

D, N Packages



BLOCK DIAGRAM



256-bit TTL bipolar RAM (256 × 1) — 82LS16

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Plastic Dual-In-Line 300mil-wide	N82LS16 N
16-Pin Plastic Small Outline 300mil-wide	N82LS16 D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage High (open-collector)	+5.5	V_{DC}
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[6]	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IH}	High	V_{CC} = 5.25V	2.0			V
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IC}	Clamp[3]	V_{CC} = 4.75V, I_{IN} = -12mA		-1.0	-1.5	V
Output voltage[2]						
		V_{CC} = 4.75V				
V_{OH}	High	I_{OH} = -3.2mA	2.6			V
V_{OL}	Low[4]	I_{OL} = 16mA		0.35	0.45	V
Input current[3]						
		V_{CC} = 5.25V				
I_{IH}	High	V_{IN} = 5.5V		1	25	µA
I_{IL}	Low	V_{IN} = 0.45V		-10	-100	µA
Output current						
I_{OZ}	Hi-Z state[5]	V_{OUT} = 5.5V		1	40	µA
		V_{OUT} = 0.45V		-1	-40	µA
I_{OS}	Short circuit[6]	V_{CC} = 5.25V, V_O = 0V	-15		-70	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V		50	70	mA
Capacitance						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time
4. Measured with a logic High stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
6. Duration of the short-circuit should not exceed 1 second.
7. I_{CC} is measured with the Write Enable and Memory Enable inputs grounded, all other inputs at 0.45V, and the output open.

256-bit TTL bipolar RAM (256 × 1) — 82LS16

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	D_{OUT}
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disable	1	X	X	Hi-Z

* "0" = All $\overline{CE}$ inputs Low; "1" = One or more $\overline{CE}$ inputs High. X = Don't care

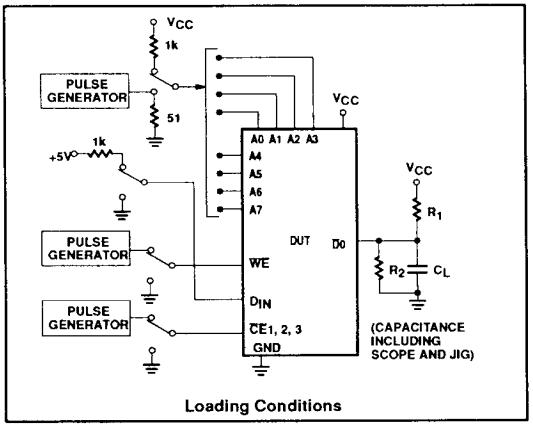
AC ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Access time							
t_{AA}	Address	Output	Address		30	40	ns
t_{CE}	Chip Enable	Output	Chip Enable		15	25	ns
Disable time[2]							
t_{CD}		Output	Chip Enable		15	25	ns
t_{WD}	Valid time	Output	Write Enable		30	40	ns
Setup and hold time							
t_{WSA}[3]	Setup time	Write Enable	Address	0	-5		ns
t_{WHA}	Hold time	Write Enable	Address	0	-5		ns
t_{WSD}	Setup time	Write Enable	Data in	25	15		ns
t_{WHD}	Hold time	Write Enable	Data in	0	-5		ns
t_{WSC}	Setup time	Write Enable	$\overline{CE}$	0	-5		ns
t_{WHC}	Hold time	Write Enable	$\overline{CE}$	0	-5		ns
Pulse width[4]							
t_{WP}[5]	Write Enable			25	15		ns

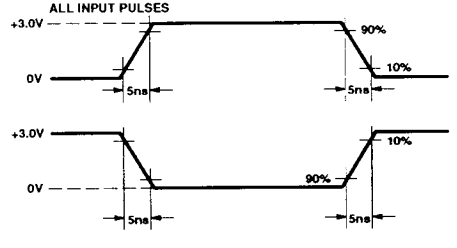
NOTES:
1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
2. Measured at a delta of 0.5V from the logic level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
3. Measured with minimum t_{WP}.
4. Minimum required to gurarantee a Write into the slowest bit.
5. Measured with minimum t_{WSA}.

TEST LOAD CIRCUIT



Loading Conditions

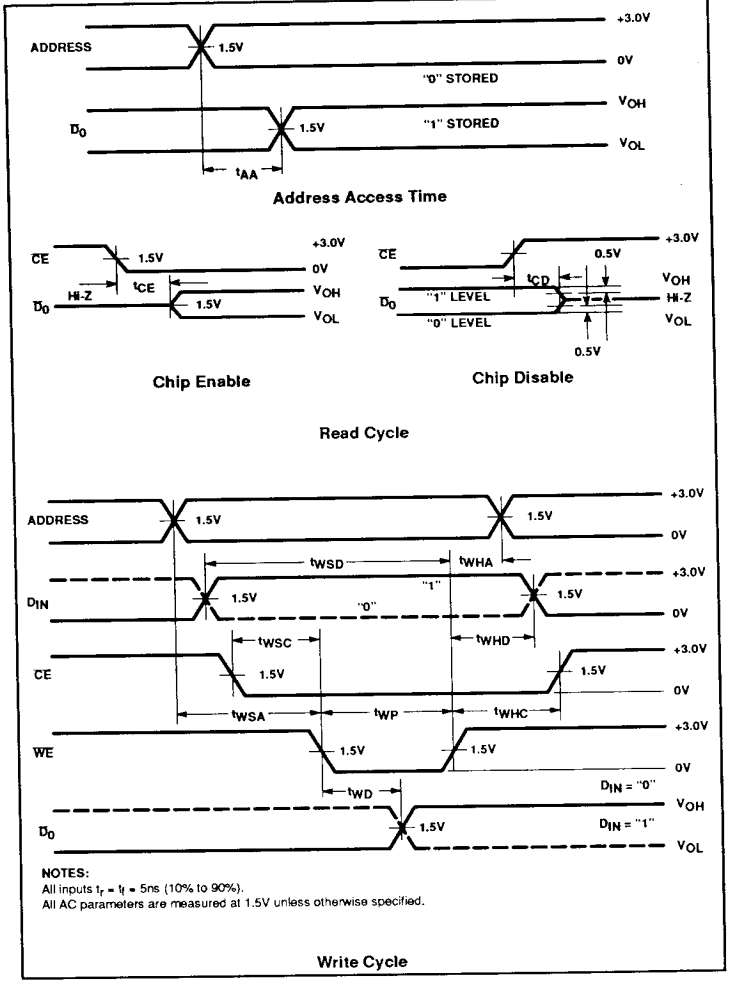
VOLTAGE WAVEFORMS



Measurements: All circuit delays are measured at the +1.5 level of inputs and output.

Input Pulses

TIMING DIAGRAMS



MEMORY TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CE}	Delay between beginning of Chip Enable Low (with Address valid) and when Data Output becomes valid.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in Off-State.
t_{AA}	Delay between beginning of valid Address (with Chip Enable Low) and when Data Output becomes valid.
t_{WSC}	Required delay between beginning of valid Chip enable and beginning of Write Enable pulse.
t_{WHD}	Required delay between end of Write Enable pulse and end of valid input data.
t_{WP}	Width of Write Enable pulse.
t_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
t_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
t_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
t_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
t_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.