

# 93422 256 x 4-Bit Static Random Access Memory

Memory and High Speed Logic

### Description

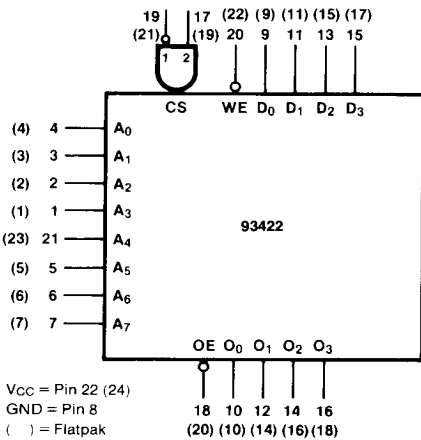
The 93422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits. It is designed for high speed cache, control and buffer storage applications. The 93422 is available in two speeds, "standard" speed and an "A" grade. The device includes full on-chip decoding, separate Data inputs and non-inverting Data outputs, as well as two Chip Select lines.

- **Commercial Address Access Time**  
93422 — 45 ns Max  
93422A — 35 ns Max
- **Military Address Access Time**  
93422 — 60 ns Max  
93422A — 45 ns Max
- **Fully TTL Compatible**
- **Features Three State Outputs**
- **Power Dissipation — 0.46 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

### Pin Names

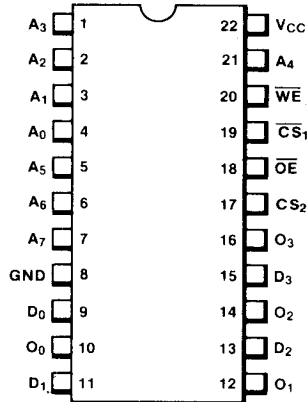
A <sub>0</sub> -A <sub>7</sub>	Address Inputs
D <sub>0</sub> -D <sub>3</sub>	Data Inputs
$\overline{CS}_1$	Chip Select Input (Active LOW)
CS <sub>2</sub>	Chip Select Input (Active HIGH)
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{OE}$	Output Enable Input (Active LOW)
O <sub>0</sub> -O <sub>3</sub>	Data Outputs

### Logic Symbol

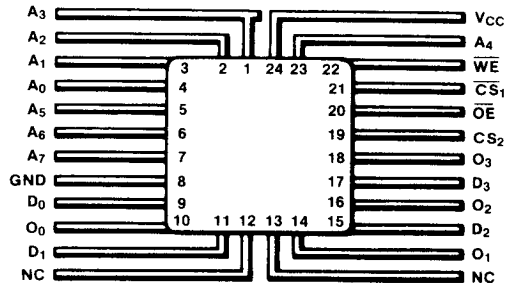


### Connection Diagrams

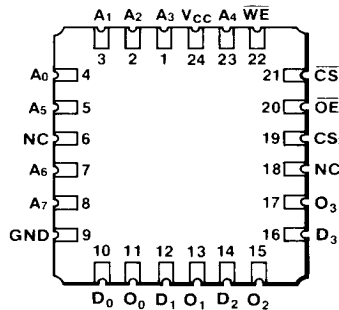
#### 22-Pin DIP (Top View)



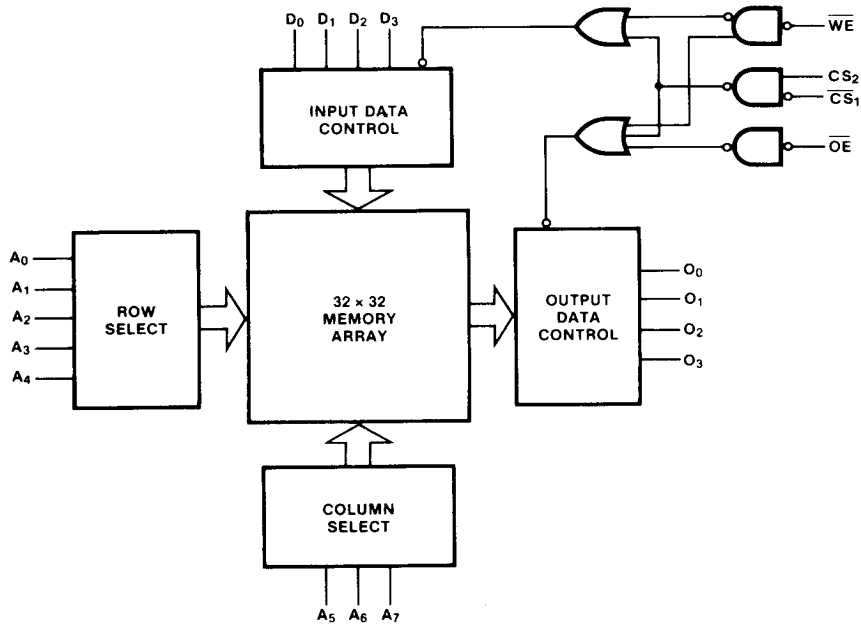
#### 24-Pin Flatpak (Top View)



#### 24-Pin Leadless Chip Carrier (Top View)



## Logic Diagram

**Functional Description**

The 93422 is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A<sub>0</sub> through A<sub>7</sub>.

Two Chip Select inputs, inverting and non-inverting, are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of the chip selects from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable ( $\overline{WE}$ ) input. When  $\overline{WE}$  is

held LOW and the chip is selected, the data at D<sub>0</sub>-D<sub>3</sub> is written into the addressed location. Since the write function is level-triggered, data must be held stable for at least  $t_{WSD(min)}$  plus  $t_{W(min)}$  plus  $t_{WHD(min)}$  to insure a valid write. To read,  $\overline{WE}$  is held HIGH and the chip selected. Non-inverted data is then presented at the outputs (O<sub>0</sub>-O<sub>3</sub>).

The 93422 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

Truth Table

Inputs				Outputs	
OE	CS <sub>1</sub>	CS <sub>2</sub>	WE	3-State	Mode
X	H	X	X	HIGH Z	Not Selected
X	X	L	X	HIGH Z	Not Selected
L	L	H	H	D <sub>OUT</sub>	READ
X	L	H	L	HIGH Z	WRITE
H	X	X	X	HIGH Z	Output Disabled

H = HIGH Voltage Level (2.4 V)

L = LOW Voltage Level (.5 V)

X = Don't Care (HIGH or LOW)

High Z = High-Impedance

**DC Performance Characteristics:** Over operating temperature ranges (Note 1)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V <sub>OL</sub>	Output LOW Voltage		0.3	0.45	V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8 mA
V <sub>IH</sub>	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for All Inputs <sup>5</sup>
V <sub>IL</sub>	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for All Inputs <sup>5</sup>
V <sub>OH</sub>	Output HIGH Voltage	2.4			V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -5.2 mA
I <sub>IL</sub>	Input LOW Current		-150	-300	μA	V <sub>CC</sub> = Max, V <sub>IN</sub> = 0.4 V
I <sub>IH</sub>	Input HIGH Current		1.0	40	μA	V <sub>CC</sub> = Max, V <sub>IN</sub> = 4.5 V
I <sub>IHB</sub>	Input Breakdown Current			1.0	mA	V <sub>CC</sub> = Max, V <sub>IN</sub> = V <sub>CC</sub>
V <sub>IC</sub>	Input Diode Clamp Voltage		-1.0	-1.5	V	V <sub>CC</sub> = Max, I <sub>IN</sub> = -10 mA
I <sub>OZH</sub> I <sub>OZL</sub>	Output Current (HIGH Z)			50 -50	μA	V <sub>CC</sub> = Max, V <sub>OUT</sub> = 2.4 V V <sub>CC</sub> = Max, V <sub>OUT</sub> = 0.5 V
I <sub>OS</sub>	Output Current Short Circuit to Ground	-10		-70	mA	V <sub>CC</sub> = Max, Note 3
I <sub>CC</sub>	Power Supply Current			120 130	mA	Commercial Military V <sub>CC</sub> = Max All Inputs GND All Outputs Open

**Notes**

- Typical values are at V<sub>CC</sub> = 5.0 V, T<sub>C</sub> = +25°C and maximum loading.
- The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
- Short circuit to ground not to exceed one second.
- t<sub>W</sub> measured at t<sub>WSA</sub> = Min. t<sub>WSA</sub> measured at t<sub>W</sub> = Min.
- Static condition only.

**Commercial****AC Performance Characteristics:**  $V_{CC} = 5.0\text{ V} \pm 5\%$ ,  $GND = 0\text{ V}$ ,  $T_C = 0^\circ\text{C to } +75^\circ\text{C}$ 

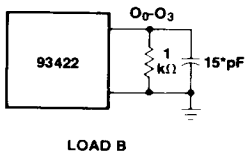
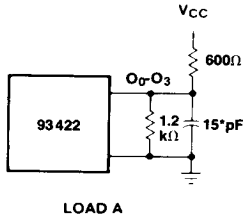
Symbol	Characteristic	A		Std		Unit	Condition
		Min	Max	Min	Max		
	<b>Read Timing</b>						
tACS	Chip Select Access Time		30		30	ns	Figures 3a, 3b, 3c
tzRCS	Chip Select to HIGH Z		30		30	ns	
tAOS	Output Enable Access Time		30		30	ns	
tzROS	Output Enable to HIGH Z		30		30	ns	
tAA	Address Access Time <sup>2</sup>		35		45	ns	
	<b>Write Timing</b>						
tw	Write Pulse Width to Guarantee Writing <sup>4</sup>	25		30		ns	Figure 4
twSD	Data Setup Time Prior to Write	5		5		ns	
twHD	Data Hold Time after Write	5		5		ns	
twSA	Address Setup Time Prior to Write <sup>4</sup>	5		5		ns	
twHA	Address Hold Time after Write	5		5		ns	
twSCS	Chip Select Setup Time Prior to Write	5		5		ns	
twHCS	Chip Select Hold Time after Write	5		5		ns	
tzWS	Write Enable to HIGH Z		35		35	ns	
tWR	Write Recovery Time		35		40	ns	

**Military****AC Performance Characteristics:**  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ ,  $T_C = -55^\circ\text{C to } +125^\circ\text{C}$ 

Symbol	Characteristic	A		Std		Unit	Condition
		Min	Max	Min	Max		
	<b>Read Timing</b>						
tACS	Chip Select Access Time		35		45	ns	Figures 3a, 3b, 3c
tzRCS	Chip Select to HIGH Z		35		45	ns	
tAOS	Output Enable Access Time		35		45	ns	
tzROS	Output Enable to HIGH Z		35		45	ns	
tAA	Address Access Time <sup>2</sup>		45		60	ns	
	<b>Write Timing</b>						
tw	Write Pulse Width to Guarantee Writing <sup>4</sup>	35		40		ns	Figure 4
twSD	Data Setup Time Prior to Write	5		5		ns	
twHD	Data Hold Time after Write	5		5		ns	
twSA	Address Setup Time Prior to Write <sup>4</sup>	5		5		ns	
twHA	Address Hold Time after Write	5		5		ns	
twSCS	Chip Select Setup Time Prior to Write	5		5		ns	
twHCS	Chip Select Hold Time after Write	5		5		ns	
tzWS	Write Enable to HIGH Z		40		45	ns	
tWR	Write Recovery Time		40		50	ns	

Notes on preceding page

Fig. 1 AC Test Output Load



\*Includes jig and probe capacitance  
 Note: Load A is used for all production testing.

Fig. 2 AC Test Input Levels

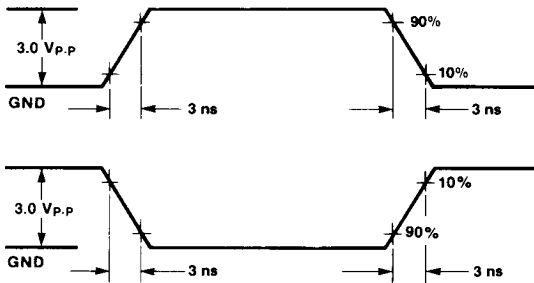
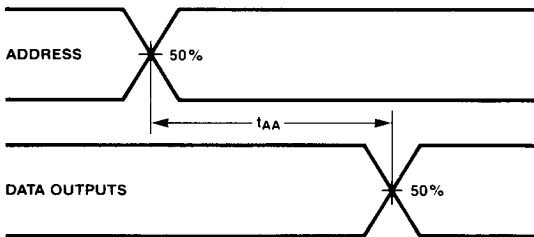
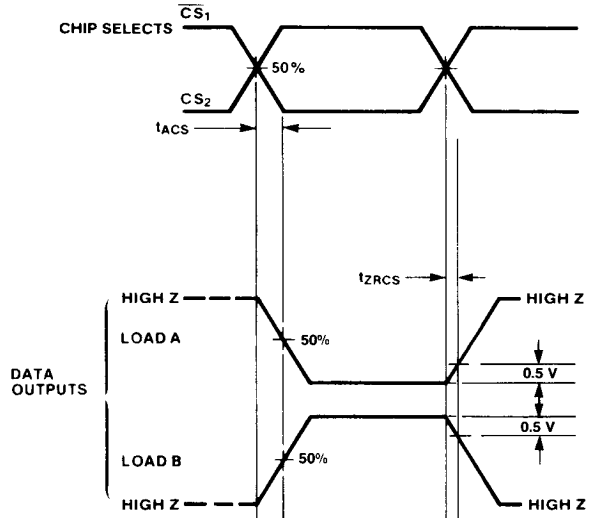


Fig. 3 Read Mode Timing

a Read Mode Propagation Delay from Address

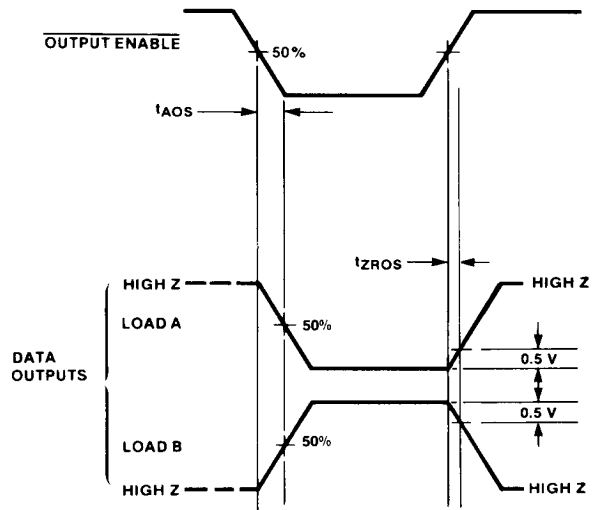


3b Read Mode Propagation Delay from Chip Select

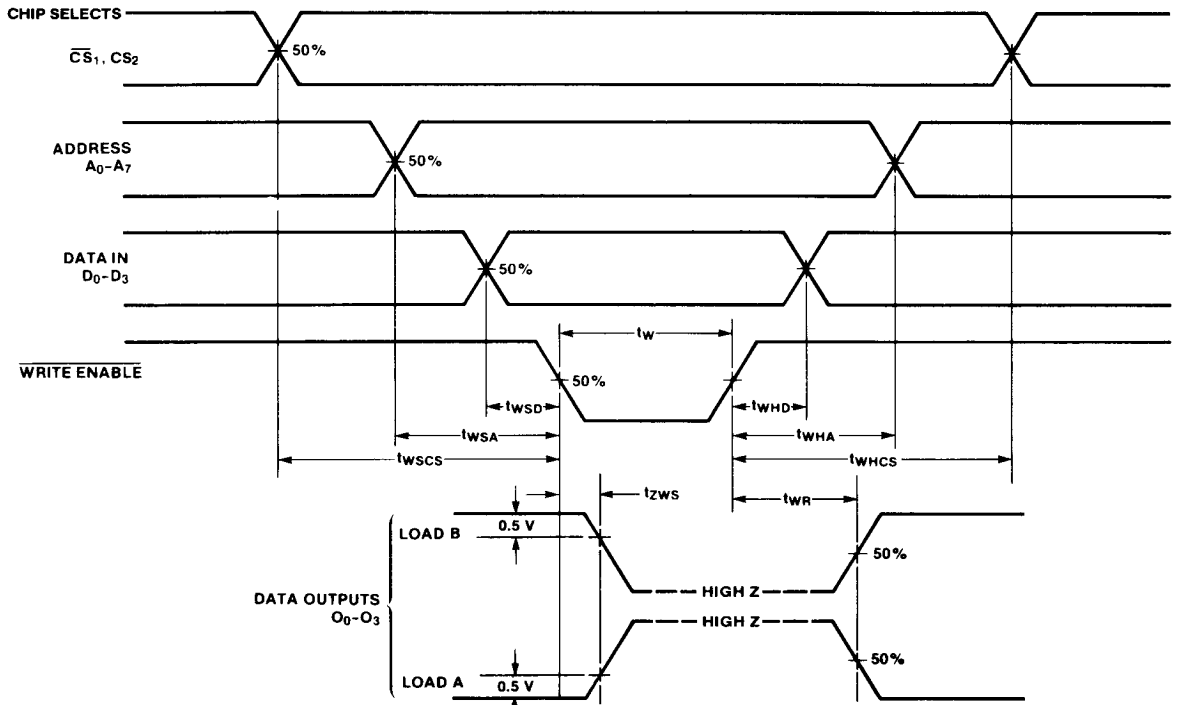


4

3c Read Mode Propagation Delay from Output Enable



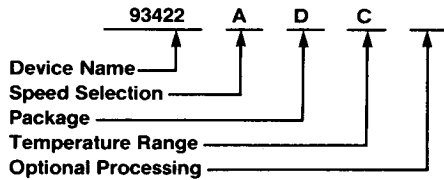
**Fig. 4 Write Mode Timing**



**Notes**

1. Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.
2. Input voltage levels for worst case AC test are 3.0/0.0 V.

**Ordering Information**



**Speed Selection**

Blank = Standard Speed  
A = 'A' Grade

**Packages and Outlines** (See Section 9)

D = Ceramic DIP  
F = Flatpak  
L = Leadless Chip Carrier  
P = Plastic DIP

**Temperature Range**

C = 0°C to +75°C  
M = -55°C to +125°C

**Optional Processing**

QB = Mil Std 883  
Method 5004 and 5005, Level B  
QR = Commercial Device with  
160 Hour Burn In or Equivalent