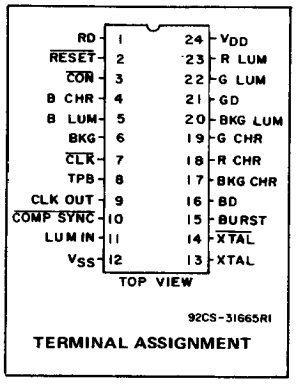
CDP1862C

Preliminary Data

CMOS Color Generator Controller



TERMINAL ASSIGNMENT

Features:

- *Interfaces directly with CDP1861C Video Display Controller*
- *Programmable background color*
- *Programmable video (dot) color*
- *On-chip crystal controlled oscillator*
- *NTSC and RGB compatible*

The RCA-CDP1862C is a color generator controller designed for use in CDP1800-series microprocessor systems. It is intended for use with the RCA-CDP1861C video display controller and will interface directly with the CDP1802/CDP1861C as shown in the system diagram below.

The CDP1862C utilizes many features of the CDP1802 and CDP1861C to simplify control and minimize the need for external components. The CDP1862C is NTSC color compatible. Red, green and blue luminance signals are also available for directly controlling the red, green and blue amplifiers of a video monitor. A 7.15909-MHz on-chip crystal-controlled oscillator or an external 7.15909-MHz clock is used to generate multiple phases of the 3.579545-MHz color burst frequency for NTSC-compatible color. The color burst is further divided by 2 to provide system timing for the CDP1802 and the CDP1861C. This frequency [1.789773 MHz] is available at CLK OUT. Two inputs TPB and COMP SYNC, are used to maintain system synchronization. The RESET input resets the CDP1862C and sets the background color to blue and the dot color to white.

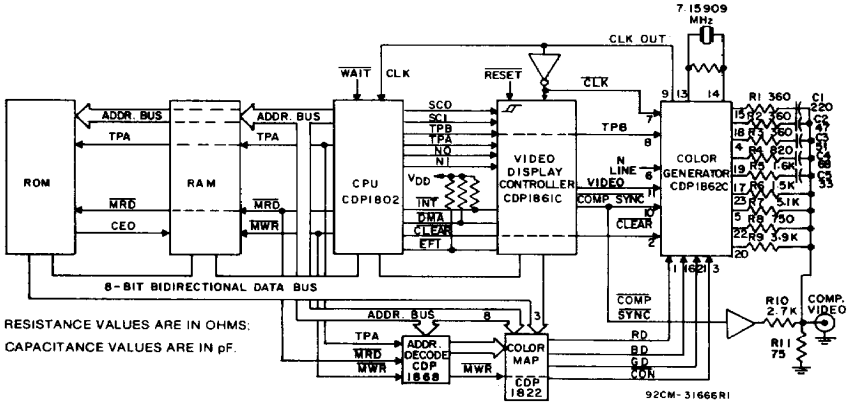


Fig. 1-Typical CDP1802 microprocessor system using the CDP1862C.

Background color: Four background colors are available. The colors are changed each time TPB is pulsed when BKG = high. The sequence is from blue to black to green to red and return to blue [see Fig. 2].

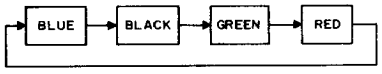


Fig. 2-Background Color Sequencing.

Dot color: Color data [RD, BD, GD] is latched internally on the high-to-low transition of $\overline{CLK}$ when TPB = high. Eight colors are available as shown in Table I. The color is overlayed onto the LUM IN data [video output from CDP1861C]. Each color

TABLE I – Color Table

RD	BD	GD	COLOR
0	0	0	Black
0	0	1	Green
0	1	0	Blue
0	1	1	Cyan
1	0	0	Red
1	0	1	Yellow
1	1	0	Purple
1	1	1	White

corresponds to eight horizontal bits of video information. Only the selected background color appears at the output if LUM IN = low. When used with the CDP1861C and set for the maximum resolution of 64 x 128, 1024 color blocks [8 x 128] are possible, and would require a 1K x 3 random-access memory storage area. This area would appear to be write-only memory to the microprocessor because, in the programmed state, this area occupies an unique, unused 1K block of memory space. However, when it is read, this area responds to the same address space occupied by the CDP1861C refresh RAM. This is accomplished with proper decoding and requires the memory to have separate I/O lines.

The $\overline{CON}$ input enables the RD, BD and GD input latches. After a $\overline{RESET}$ condition, the dot color is set to white and any color change is inhibited until the $\overline{CON}$ input is pulsed low, which normally occurs when data is written into the color map. The $\overline{CON}$ input provides a means of inhibiting erroneous color data until the color map is properly loaded.

The color luminance [R LUM, B LUM, G LUM], color chrominance [R CHR, B CHR, G, CHR], background luminance [BKG LUM], background chrominance [$\overline{BKG\ CHR}$], color burst [BURST], and $\overline{COMP\ SYNC}$ are combined by an external RC network to generate the composite video [see Fig. 1].

The BURST signal is normally high and oscillates at ½ the XTAL frequency from the low-to-high transition of $\overline{COMP\ SYNC}$ until TPB = high.

The CDP1862C types are supplied in 24-lead hermetic dual-in-line side-brazed ceramic packages [D suffix], and in 24-lead dual-in-line plastic packages [E suffix].

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	–	4	6.5	V
Input Voltage Range	–	V_{SS}	V_{DD}	
Input Signal Rise or Fall Time, t_r, t_f	5	–	5	μs
Clock Input Frequency, f_{CL}	5	7.15909		MHz

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPE D) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, except as noted.

CHARACTERISTIC	CONDITIONS			LIMITS			UNITS
				CDP1862CD CDP1862CE			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	
Quiescent Device Current, I_L	–	0, 5	5	–	50	250	μA
Output Low Drive (Sink) Current, I_{OL} (Except $\overline{XTAL}$)	0.4	0, 5	5	2	2.4	–	mA
$\overline{XTAL}$ Output, I_{OL}	0.4	0, 5	5	150	200	–	μA
Output High Drive (Source) Current, I_{OH} (Except $\overline{XTAL}$	4.6	0, 5	5	−1.6	−1.8	–	mA
$\overline{XTAL}$ Output, I_{OH}	4.6	0, 5	5	−150	−200	–	μA
Output Voltage Low-Level, V_{OL}	–	0, 5	5	–	0	0.1	V
Output Voltage High Level, V_{OH}	–	0, 5	5	4.9	5	–	
Input Low Voltage, V_{IL}	0.5, 4.5	–	5	–	–	1.5	
Input High Voltage, V_{IH}	0.5, 4.5	–	5	3.5	–	–	
Input Leakage Current, I_{IN}	Any Input	0, 5	5	–	±0.1	±1	μA

* Typical values are for T_A = 25°C and nominal voltage.

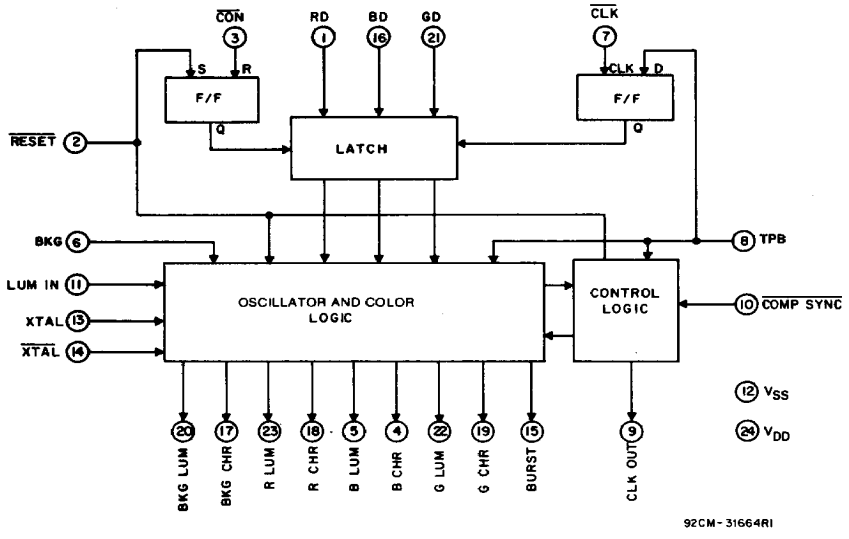


Fig. 3-Functional block diagram.

SIGNAL DESCRIPTIONS

RESET

A low level on this input initializes the internal counters, sets the background color to blue, and sets the dot color to white.

BKG

A high level on this input enables the background color to be changed when TPB is pulsed high. This signal is normally connected to an I/O line of the 1800-Series microprocessor.

CLK

An input signal used to latch the color data information. Color data [RD, BD, GD] is latched on the high-to-low transition of CLK when TPB = high. This signal is normally connected to CLK OUT through an inverter.

TPB

A high level on this input enables color data latching and sequences background color when BKG = high. This signal is normally connected to the TPB terminal of the 1800-Series microprocessor.

CLK OUT

An output signal, equal to the XTAL frequency divided by four, that provides the overall system synchronization. This signal is normally connected to the CLOCK terminal of the 1800-Series microprocessor. The inverse of this signal is normally connected to the CLOCK terminal of the CDP1861C and the CLK terminal of the CDP1862C.

COMP SYNC

An input signal used to provide horizontal line synchronization between the CDP1861C and the CDP1862C color signals. This signal is normally connected to the COMP SYNC terminal of the CDP1861C.

LUM IN

The luminance video input, to which the color information is added. One color block corresponds to eight serial bits of data from this input. This input is normally connected to the VIDEO terminal of the CDP1861C.

VSS

Negative supply voltage; ground.

XTAL, XTAL

Terminal connections for an external crystal, in parallel with a resistance [10 megohms typ.] if the on-chip oscillator is utilized. Frequency trimming capacitors may be required at terminals 13 and 14. XTAL is the input for an externally generated single-phase clock.

BURST

The color reference output, which oscillates at the XTAL frequency divided by 2.

This signal provides approximately 11 cycles of 3.579545 MHz from the low-to-high transition of $\overline{\text{COMP SYNC}}$ until TPB = high. This signal is coupled through an external series RC circuit to the $\overline{\text{COMP SYNC}}$ output of the CDP1861C.

RD, BD, GD
The red, blue, and green color data inputs. One of eight colors is latched on the high-to-low transition of $\overline{\text{CLK}}$ when TPB = high, forming a color block of eight horizontal LUM IN data bits. Only the selected background color appears at the output if LUM IN = low. These inputs are normally connected to the DATA OUT terminals of the color map memory.

BKG LUM, R LUM, B LUM, G LUM
These output signals provide background and color luminance information. They are resistively added externally to the $\overline{\text{COMP SYNC}}$ output of the CDP1861C.

BKG CHR, R CHR, B CHR, G CHR
These output signals provide background and color chrominance information. They are coupled through an external series RC circuit to the $\overline{\text{COMP SYNC}}$ output of the CDP1861C. Each signal is phase-shifted from the BURST reference signal by the amount necessary for proper color operation.

$\overline{\text{CON}}$
The color data input latch enable signal. After a $\overline{\text{RESET}}$ condition, the internal RD, BD, and GD input latches are held in a reset state, providing a white color output. When $\overline{\text{CON}}$ is pulsed low, the reset state is removed and the latches are enabled, providing color output. This input is normally connected to the gated $\overline{\text{MWR}}$ signal from the 1800-Series Microprocessor.

VDD
Positive supply voltage.

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. **Operating**

Operating Voltage
During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD}-V_{SS} to exceed the absolute maximum rating.

Input Signals
To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs
A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits
Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.