Signetics

AN101

T-51-09-03

Applying the DAC08

Application Note

Linear Products

Reference Amplifier Setup

The DAC08 Series are multiplying D-to-A converters in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full-scale output current is a linear function of the reference current and is given by this equalization where $I_{REF} = I_{14}$.

$$I_{FS} = \frac{255}{256} \times I_{REF}$$

In positive reference applications shown in Figure 1, an external positive reference voltage forces current through R14 into the V_{REF} (+) terminal (Pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to V_{REF} (–) at Pin 15, shown in Figure 2. Reference current flows from ground through R14 into $V_{REF}(+)$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at Pin 15. The voltage at Pin 14 is equal to and tracks the voltage at Pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors. R15 may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or Pin 15 as shown in Figure 3. The negative common-mode range of the reference amplifier is given by the following equation:

$$V_{CM-} = V- + (I_{REF} \cdot 1k\Omega) + 2.5V$$

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into 2 resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications, a +10.0V reference is recommended for optimum full-scale temperature coefficient performance. This will minimize the contributions of reference amplifier V_{OS} and TCV_{OS}. For most applications, the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14. An improved method of full-scale trimming which eliminates potentiometer TC effects is shown in Figure 4.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common-mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from Pin 16 to V–. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications".

Multiplying Operation

The DAC08 Series provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4mA to 4μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA.

Reference Amplifier Compensation for Multiplying Applications

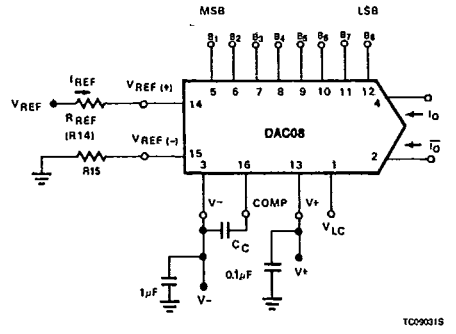
AC reference applications will require the reference amplifier to be compensated using a capacitor from Pin 16 to V–. The value of this capacitor depends on the impedance presented to Pin 14. For R14 values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37 and 75pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin.

For fastest multiplying response, low values of R14 enabling small C_C values should be used. If Pin 14 is driven by a high impedance such as a transistor current source, none of the preceding values will suffice and the amplifier must be heavily compensated, which will decrease overall bandwidth and slew rate. For R14 = 1kΩ and CC = 15pF, the reference amplifier slews at 4mA/μs enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2mA$ in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme shown in Figure 5. This technique provides lowest full-scale transition times. Full-scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at Pin 14 is 200Ω and $C_C = 0$. This yields a reference slew rate of 16mA/μs, which is relatively independent of R_{IN} and V_{IN} values.

Logic Inputs

The DAC08 design incorporates a logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V– = –15V, the logic inputs may swing between –11V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC08 is pow-



NOTES:

$I_{FS} \approx + \frac{V_{REF}}{R_{REF}} \times \frac{255}{256}$ $I_O + \overline{I_O} = I_{FS}$ for all logic states

For fixed reference, TTL operation typical values are:
$V_{REF} = +10.000V$, $R_{REF} = 5{,}000\Omega$, $R15 \approx R_{REF}$,
$C_C = 0.01\mu F$, $V_{LC} = 0V$(ground)

Figure 1. Basic Positive Reference Operation

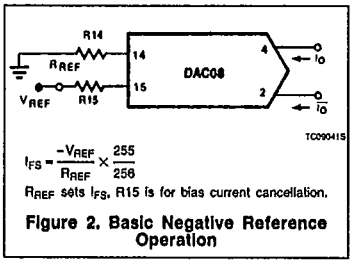
Applying the DAC08

AN101

T-51-09-03

ered from a +5V supply. Minimum input logic swing is given by the following equation:

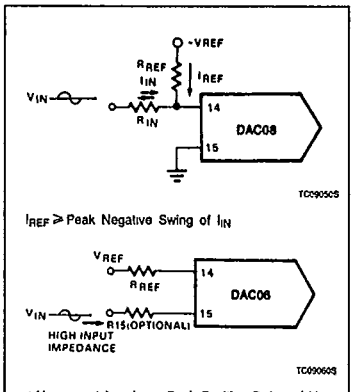
$V- + (I_{REF} \cdot 1k\Omega) + 2.5V$



$I_{FS} = \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$

R_{REF} sets I_{FS}. R15 is for bias current cancellation.

Figure 2. Basic Negative Reference Operation



$+V_{REF}$ must be above Peak Positive Swing of V_{IN}

Figure 3. Accomodating Bipolar References

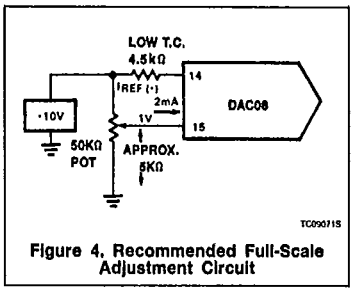


Figure 4. Recommended Full-Scale Adjustment Circuit

The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control in (Pin 1, V_{LC}). Figure 6 shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL and DTL interface, simply ground Pin 1. When interfacing ECL, an I_{REF} = 1mA is recommended. For interfacing other logic families, see Figure 7. For general setup of the logic control circuit, it should be noted that Pin 1 may source up to 200μA. External circuitry should be designed to accommodate this current.

Fastest settling times are obtained when Pin 1 sees a low impedance. If Pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

Analog Output Currents

Both true and complemented output sink currents are provided, where $I_O + \overline{I_O} = I_{FS}$. Current appears at the true output when a 1 is applied to each logic input. As the binary count increases, the sink current at Pin 4 increases proportionally, in the fashion of a positive logic D-to-A converter. When a 0 is applied to any input bit, that current is turned off at Pin 4 and turned on at Pin 2. A decreasing logic count increases I_O as in a negative or inverted logic D-to-A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}. Do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V- and is independent of the positive supply. Negative compliance is given by the equation:

$V- + (I_{REF} \cdot 1k\Omega) + 3.0V$

Note that lower values of I_{REF} will allow a greater output compliance.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as balanced-bridge A/D circuits, as well as driving center-tapped coils and transformers.

Power Supplies

The DAC08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq 1mA$ is recommended.

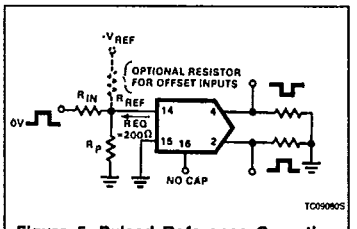


Figure 5. Pulsed Reference Operation

Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range. Consult the various figures for guidance. For example, operation at -4.5V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible; however, at least 8V total must be applied between Pins 2 and 4, and Pin 3 to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be useful to insure logic swings, etc., remain between acceptable limits.

Power consumption may be calculated by this equation:

$P_D = (I+)(V+) + (I+)(V-) + (I_{REF})(V-)$

A useful feature of the DAC08 design is that supply current is constant and independent of input logic states. This is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

Temperature Performance

The linearity and monotonicity specifications of the DAC08 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is low, typically ±10ppm/°C with zero-scale output current and drift essentially negligible compared to ½ LSB.

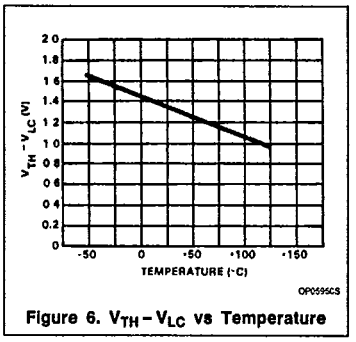


Figure 6. $V_{TH} - V_{LC}$ vs Temperature

Full-scale output drift performance will be best with +10.0V references, as V_{OS} and TCV_{OS} of the reference amplifier will be very small compared to 10.0V. The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full-scale drift.

5

Applying the DAC08

AN101

T-51-09-03

Settling times of the DAC08 decrease approximately 10% at −55°C, and an increase of about 15% at +125°C is typical.

Settling Time

The DAC08 is capable of extremely fast settling times (typically 70ns at I_{REF} = 2.0mA).

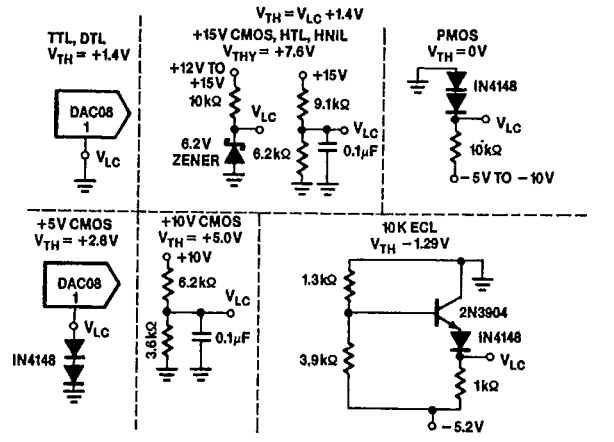
Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35ns for each of the 8 bits. Settling time to within ½ LSB is therefore 35ns, with each progressively larger bit taking successively longer. The MSB settles in 70ns, thus determining the overall settling time of 70ns. Settling to 6-bit accuracy requires about 55 to 60ns. The output capacitance, including the package, is approximately 15pF. Therefore, the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4μA. Therefore, a 1kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of Figure 8 uses a cascode design to permit driving a 1kΩ load with less than 5pF of parasite capacitance at the measurement node. At I_{REF} values of less than 1.0mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value; thus, settling time may be observed at lower values of I_{REF}.

The DAC08 switching transients or glitches are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is dependent of input logic states. 0.1μF capacitors at the supply pins provide full transient performance.



NOTE:
Do not exceed negative logic input range of DAC

Figure 7. Interfacing With Various Logic Families

Applying the DAC08

AN101

T-51-09-03

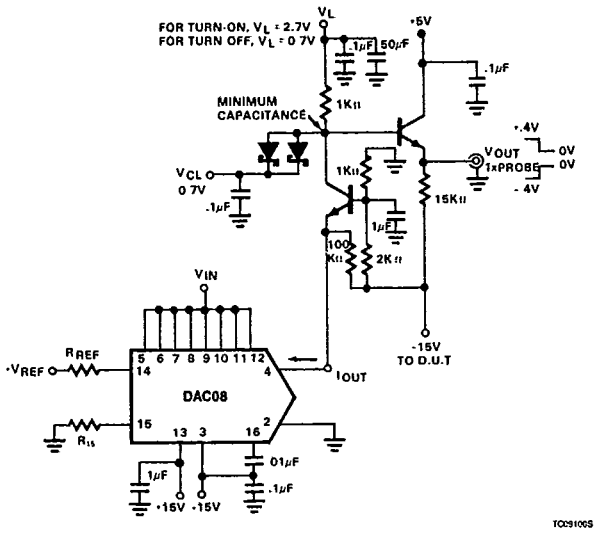
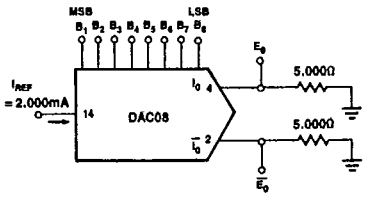


Figure 8. Settling Time Measurement

TYPICAL APPLICATIONS



	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	I_O (mA)	$\overline{I_O}$ (mA)	E_O	$\overline{E_O}$
Full-scale	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
Full-scale − LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	−0.040
Half-scale + LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
Half-scale	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
Half-scale − LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
Zero-scale + LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
Zero-scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

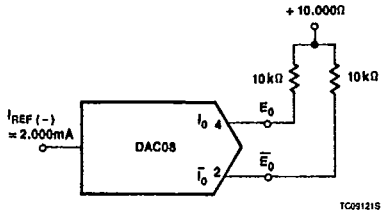
Figure 9. Basic Unipolar Negative Operation

5

Applying the DAC08 AN101

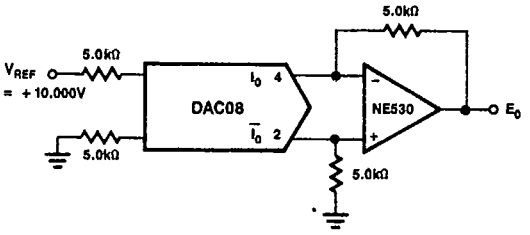
T-51-09-03

TYPICAL APPLICATIONS (Continued)



	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	E_O	$\bar{E}_O$
Pos full-scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos full-scale − LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero-scale + LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero-scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero-scale − LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg full-scale + LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg full-scale	0	0	0	0	0	0	0	0	+10.000	−9.920

Figure 10. Basic Bipolar Output Operation

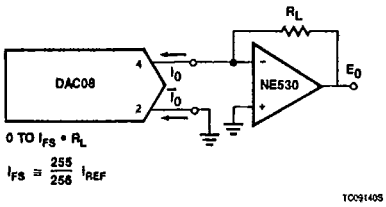


	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	E_O
Pos full-scale	1	1	1	1	1	1	1	1	+9.920
Pos full-scale − LSB	1	1	1	1	1	1	1	0	+9.840
(+) Zero-scale	1	0	0	0	0	0	0	0	+0.040
(−) Zero-scale	0	1	1	1	1	1	1	1	−0.040
Neg full-scale + LSB	0	0	0	0	0	0	0	1	−9.840
Neg full-scale	0	0	0	0	0	0	0	0	−9.920

Figure 11. Symmetrical Offset Binary Operation

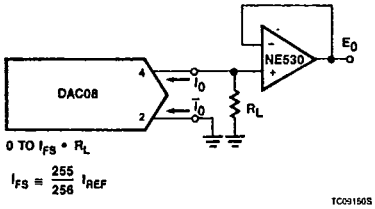
Applying the DAC08 AN101

T-51-09-03



NOTE:
For complementary output (operation as negative logic DAC), connect inverting input of op amp to I_0 (Pin 2); connect $\overline{I_0}$ (Pin 4) to ground.

Figure 12. Positive Low Impedance Output Operation



NOTE:
For complementary output (operation as a negative logic DAC), connect non-inverting input of op amp to I_0 (Pin 2); connect $\overline{I_0}$ (Pin 4) to ground.

Figure 13. Negative Low Impedance Output Operation

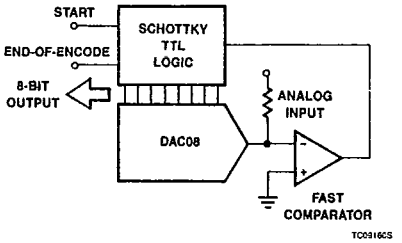
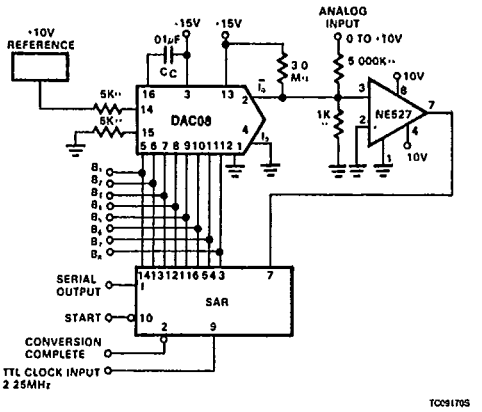


Figure 14. Low Cost 8-Bit 1μs A-to-D Converter

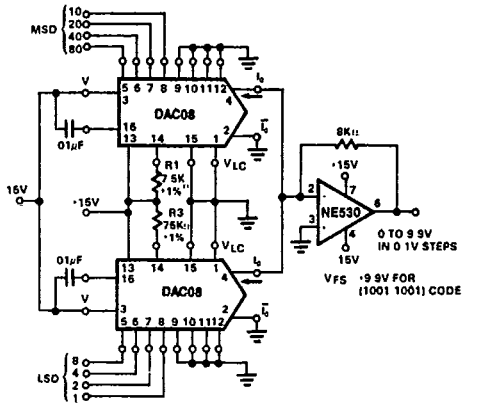
Applying the DAC08 AN101

T-51-09-03



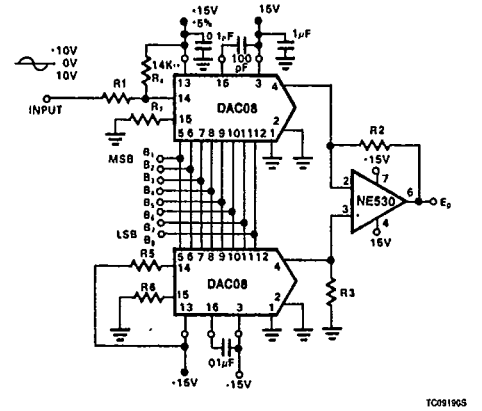
NOTE:
Connect "start" to "conversion complete" for continuous conversions.

Figure 15. 3 IC Low Cost A-to-D Converter



NOTE:
Output is directly proportional to positive power supply.

Figure 16. Low Cost 2-Digit BCD DAC



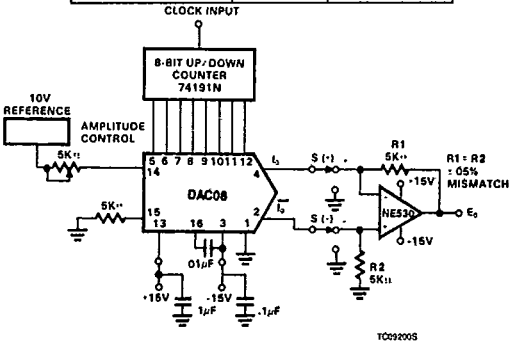
Bipolar input offset binary output

Performs 2 quadrant multiplications — AC input controls output polarity.

NOTES:
1. R1 = R2 = R3
2. R4 = R5
3. E_O DC to 20kHz = ±5V
4. E_O DC to 10kHz = ±10V

Figure 17. DC-Coupled Digital Attenuator/ Programmable Gain Amplifier

OUTPUT TYPE (E_O)	SWITCH S(+)	CONDITIONS S(-)
Unipolar positive	+	GND
Unipolar negative	GND	-
Bipolar	+	-



NOTES:
1. Bipolar output is symmetrical around zero, adjustable peak-to-peak amplitude.
2. For triangle wave, count up to full, reverse and count down.
3. For positive-going sawtooth, count up to full, clear, repeat.
4. For negative-going sawtooth, count down, clear, repeat.
5. For other waveforms, use a ROM programmed with the desired function.

Figure 18. High-Speed Waveform Generator