DAC-08

8-Bit High Speed Multiplying D/A Converter

Distinctive Characteristics

- Fast settling output current — 85nsec
- Full scale current prematched to ±1.0 LSB
- Direct interface to TTL, CMOS, ECL, HTL, NMOS
- Nonlinearity to ±0.1% max over temperature range
- High output impedance and compliance
  −10V to +18V
- Differential current outputs
- Wide range multiplying capability
  1.0MHz bandwidth
- Low FS current drift — ±10ppm/°C
- Wide power supply range — ±4.5V to ±18V
- Low power consumption — 33mW @ ±5V

GENERAL DESCRIPTION

The DAC-08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85 nsec settling times with very low "glitch" and a low power consumption. Monotonic multiplying performance is attained over more than a 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

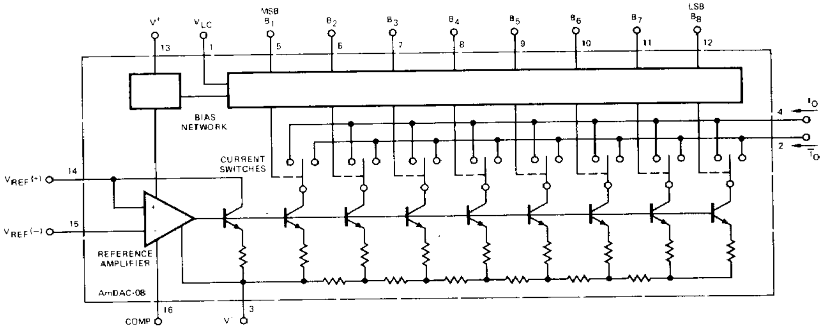
High voltage compliance dual complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 33mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications. All devices are processed to MIL-STD-883.

DAC-08 applications include 8-bit, 1.0μsec A/D converters, servo-motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high speed modems and other applications where low cost, high speed and complete input/output versatility are required.

EQUIVALENT CIRCUIT



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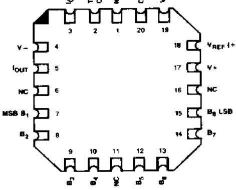
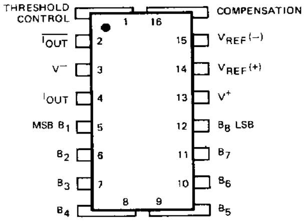
CONNECTION DIAGRAMS – Top Views

Leadless Chip-Pak
L-20-1



P-16-1
D-16-1



Note: Pin 1 is marked for orientation.

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DAC-08

MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

Operating Temperature	
DAC-08AQ, Q, AL, L	−55°C to +125°C
DAC-08EQ, CQ, HQ, EN, CN, HN	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation	500mW
Derate above 100°C	10mW/°C
Lead Temperature (Soldering, 60 sec)	300°C

V+ supply to V− Supply	36V
Logic Inputs	V− to V+ plus 36V
V_{LC}	V− to V+
Analog Current Outputs	See Fig. 12
Reference Inputs (V_{14}, V_{15})	V− to V+
Reference Input Differential Voltage (V_{14} to V_{15})	±18V
Reference Input Current (I_{14})	5.0mA

ELECTRICAL CHARACTERISTICS (V_S = ±15V, I_{REF} = 2.0mA)

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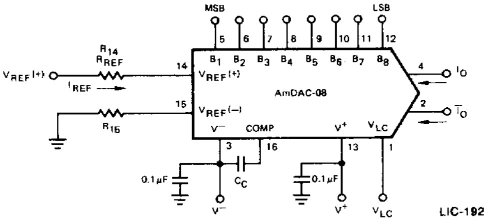
Parameter	Description		Test Conditions		AmDAC-08A AmDAC-08H			AmDAC-08 AmDAC-08E			AmDAC-08C			Units
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
	Resolution				8	8	8	8	8	8	8	8	8	Bits
	Monotonicity				8	8	8	8	8	8	8	8	8	Bits
	Nonlinearity		T_A = MIN. to MAX.				±0.1			±0.19			±0.39	%FS
t_s	Settling Time		To ±1/2 LSB, all bits switched ON or OFF T_A = 25°C	DAC-08A DAC-08		85	135		85	135				ns
				DAC-08E DAC-08C					85	150		85	150	
t_{PLH}, t_{PHL}	Propagation Delay	Each Bit	T_A = 25°C			35	60		35	60		35	60	ns
		All Bits Switched				35	60		35	60		35	60	
TCI_{FS}	Full Scale Tempco					±10	±50		±10	±50		±10	±80	ppm/°C
V_{OC}	Output Voltage Compliance		Full scale current change < 1/2 LSB R_{OUT} > 20MegΩ typ.		−10		+18	−10		+18	−10		+18	Volts
I_{FS4}	Full Scale Current		V_{REF} = 10.000V R_{14}, R_{15} = 5.000kΩ T_A = 25°C		1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full Scale Symmetry		$I_{FS4} - I_{FS2}$			±0.5	±4.0		±1.0	±8.0		±2.0	±16	μA
I_{ZS}	Zero Scale Current					0.1	1.0		0.2	2.0		0.2	4.0	μA
I_{FSR}	Output Current Range		V^- = −5.0V		0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
			V^- = −12.0V to −18V		0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	
V_{IL}	Logic Input Levels	Logic "0"	V_{LC} = 0V				0.8			0.8			0.8	Volts
V_{IH}		Logic "1"			2.0			2.0			2.0			
I_{IL}	Logic Input Current	Logic "0"	V_{LC} = 0V	V_{IN} = −10V to +0.8V		−2.0	−10		−2.0	−10		−2.0	−10	μA
I_{IH}		Logic "1"		V_{IN} = 2.0V to 18V		0.002	10		0.002	10		0.002	10	
V_{IS}	Logic Input Swing		V^- = −15V		−10		+18	−10		+18	−10		+18	Volts
V_{THR}	Logic Threshold Range		V_S = ±15V		−10		+13.5	−10		+13.5	−10		+13.5	Volts
I_{15}	Reference Bias Current					−1.0	−3.0		−1.0	−3.0		−1.0	−3.0	μA
dI/dt	Reference Input Slew Rate				4.0	8.0		4.0	8.0		4.0	8.0		mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity		V^+ = 4.5V to 18V			±0.0003	±0.01		±0.0003	±0.01		±0.0003	±0.01	%/%
$PSSI_{FS-}$			V^- = −4.5V to −18V I_{REF} = 1.0mA			±0.002	±0.01		±0.002	±0.01		±0.002	±0.01	
I^+	Power Supply Current		V_S = ±5.0V, I_{REF} = 1.0mA			2.3	3.8		2.3	3.8		2.3	3.8	mA
I^-						−4.3	−5.8		−4.3	−5.8		−4.3	−5.8	
I^+			V_S = +5.0V, −15V, I_{REF} = 2.0mA			2.4	3.8		2.4	3.8		2.4	3.8	
I^-						−6.4	−7.8		−6.4	−7.8		−6.4	−7.8	
I^+			V_S = ±15V, I_{REF} = 2.0mA			2.5	3.8		2.5	3.8		2.5	3.8	
I^-						−6.5	−7.8		−6.5	−7.8		−6.5	−7.8	
P_D	Power Dissipation		±5.0V, I_{REF} = 1.0mA			33	48		33	48		33	48	mW
			+5.0V, −15V, I_{REF} = 2.0mA			108	136		108	136		108	136	
			±15V, I_{REF} = 2.0mA			135	174		135	174		135	174	

BASIC CONNECTIONS



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$$I_{FS} = \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \overline{I_O} = I_{FS}$ FOR ALL LOGIC STATES

FOR FIXED REFERENCE, TTL OPERATION, TYPICAL VALUES ARE:

$V_{REF} = +10.000V$
$R_{REF} = 5.000k$
$R_{15} \approx R_{REF}$
$C_C = 0.01\mu F$
$V_{LC} = 0V$ (GROUND)

Figure 1. Basic Positive Reference Operation.

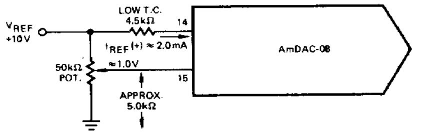

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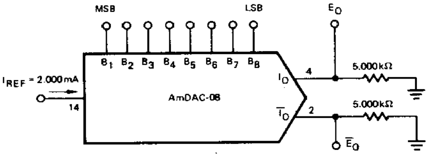
Figure 2. Recommended Full Scale Adjustment Circuit.

LIC-194

$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

Note 1. R_{REF} Sets I_{FS}; R_{15} is for Bias Current Cancellation.

Figure 3. Basic Negative Reference Operation.



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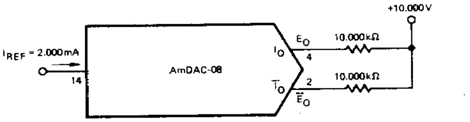
	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
FULL SCALE	1	1	1	1	1	1	1	1	1.992	000	−9.960	000
FULL SCALE −LSB	1	1	1	1	1	1	1	0	1.984	.008	−9.920	−.040
HALF SCALE +LSB	1	0	0	0	0	0	0	1	1.008	.984	−5.040	−4.920
HALF SCALE	1	0	0	0	0	0	0	0	1.000	.992	−5.000	−4.960
HALF SCALE −LSB	0	1	1	1	1	1	1	1	.992	1.000	−4.960	−5.000
ZERO SCALE +LSB	0	0	0	0	0	0	0	1	.008	1.984	−.040	−9.920
ZERO SCALE	0	0	0	0	0	0	0	0	.000	1.992	.000	−9.960

Figure 4. Basic Unipolar Negative Operation.



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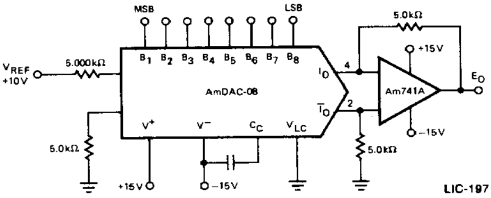
	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
POS FULL SCALE	1	1	1	1	1	1	1	1	−9.920	+10.000
POS FULL SCALE −LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
ZERO SCALE +LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	+0.080
ZERO SCALE −LSB	0	1	1	1	1	1	1	1	+0.080	0.000
NEG FULL SCALE +LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	+10.000	−9.920

Figure 5. Basic Bipolar Output Operation.



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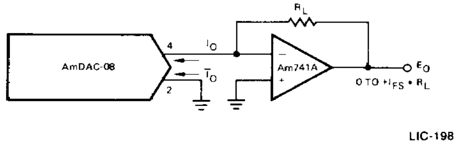
	B1	B2	B3	B4	B5	B6	B7	B8	E_O
POS FULL SCALE	1	1	1	1	1	1	1	1	+9.960
POS FULL SCALE −LSB	1	1	1	1	1	1	1	0	+9.880
(+) ZERO SCALE	1	0	0	0	0	0	0	0	+0.040
(−) ZERO SCALE	0	1	1	1	1	1	1	1	−0.040
NEG FULL SCALE +LSB	0	0	0	0	0	0	0	1	−9.880
NEG FULL SCALE	0	0	0	0	0	0	0	0	−9.960

Figure 6. Symmetrical Offset Binary Operation.

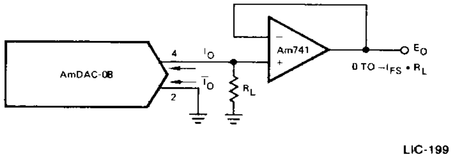
BASIC CONNECTIONS (Cont.)



$$I_{FS} \cong \frac{255}{256} I_{REF}$$

FOR COMPLEMENTARY OUTPUT (OPERATION AS NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2), CONNECT I_O (PIN 4) TO GROUND

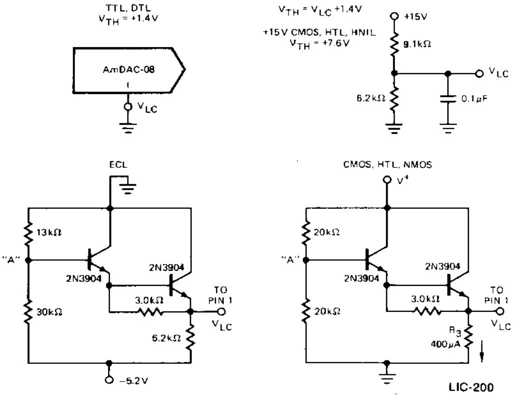
Figure 7. Positive Low Impedance Output Operation.



$$I_{FS} \cong \frac{255}{256} I_{REF}$$

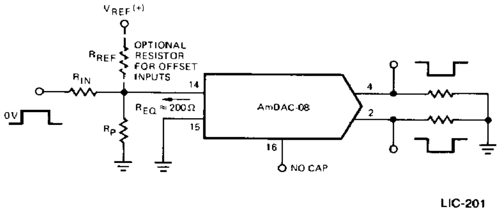
FOR COMPLEMENTARY (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

Figure 8. Negative Low Impedance Output Operation.



SET VOLTAGE AT NODE "A" EQUAL TO DESIRED LOGIC THRESHOLD.

Figure 9. Interfacing With Various Logic Families.

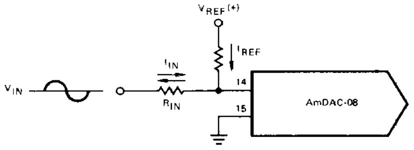


TYPICAL VALUES:

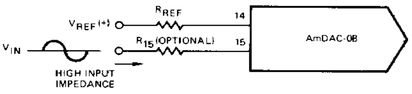
R_{IN} = 5k

$+V_{IN}$ = 10V

Figure 10. Pulsed Reference Operation.



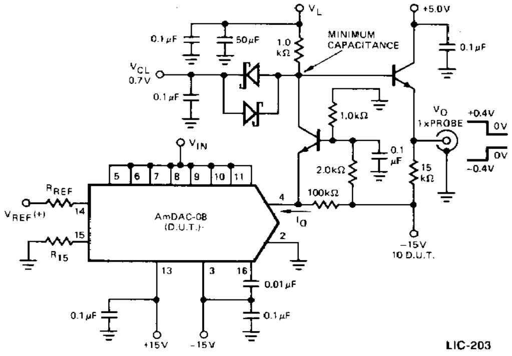
a) $I_{REF} \geqslant$ Peak Negative Swing of I_{IN}.



$R_{REF} \approx R_{15}$ LIC-202

b) $+V_{REF}$ Must Be Above Peak Positive Swing of V_{IN}.

Figure 11. Accomodating Bipolar References.



FOR TURN-ON, V_L = 2.7V

FOR TURN-OFF, V_L = 0.7V

Figure 12. Settling Time Measurement.

APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SET-UP

The DAC-08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full scale output current is a linear function of the reference current and is given by:

$$I_{FS} = \frac{255}{256} \times I_{REF} \text{ where } I_{REF} = I_{14}.$$

In positive reference applications (Fig. 1), an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15 (Fig. 3); reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors; R_{15} may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15 as shown in Fig. 11. The negative common mode range of the reference amplifier is given by: $V_{CM-} = V-$ plus ($I_{REF} \times 1.0k\Omega$) plus 2.5V. The positive common mode range is V+ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications, a +10.0V reference is recommended for optimum full scale temperature coefficient performance. This will minimize the contributions of reference amplifier V_{OS} and TCV_{OS}. For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}. An improved method of full scale trimming which eliminates potentiometer T.C. effects is shown in Fig. 2.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 16 to V−. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

MULTIPLYING OPERATION

The DAC-08 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4.0mA to 4.0μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA; consult factory for devices selected for monotonic operation over wider I_{REF} ranges.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the impedance presented to pin 14: for R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37, and 75pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14} = 1.0kΩ and C_C = 15pF, the reference amplifier slews at 4.0mA/μs enabling a transition from $I_{REF} = 0$ to I_{REF} = 2.0mA in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme shown in Fig. 10. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. Full scale transition (0 to 2.0mA) occurs in 120ns when the equivalent impedance at pin 14 is 200Ω and $C_C = 0$. This yields a reference slew rate of 16mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2.0μA logic input current and completely adjustable logic threshold voltage. For V− = −15V, the logic inputs may swing between −10V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V− plus ($I_{REF} \times 1.0k\Omega$) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an I_{REF} = 1.0mA is recommended. For interfacing other logic families, see Fig. 9. For general set-up of the logic control circuit, it should be noted that pin 1 will source 100μA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1.0kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided, when $I_O + \overline{I_O} = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V− and is independent of the positive supply. Negative compliance is given by V− plus ($I_{REF} \cdot 1.0k\Omega$) plus 2.5V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leqslant 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range. For example, operation at −4.5V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required: however, an artificial ground may be useful to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows:

$P_d = (I+)\ (V+) + (I+)\ (V-) + (2\ I_{REF})\ (V-)$. A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-08 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is tight, typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

Full scale output drift performance will be best with +10.0V references as V_{OS} and TCV_{OS} of the reference amplifier will be very small compared to 10.0V. The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full scale drift. Settling times of the DAC-08 decrease approximately 10% at −55°C; at +125°C an increase of about 15% is typical.

SETTLING TIME

The DAC-08 is capable of extremely fast settling times, typically 85nsec at I_{REF} = 2.0mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35nsec for each of the 8 bits. Settling time to within 1/2 LSB of the LSB is therefore 35nsec, with each progressively larger bit taking successively longer. The MSB settles in 85nsec, thus determining the overall settling time of 85nsec. Settling to 6-bit accuracy requires about 65 to 70nsec. The output capacitance of the DAC-08 including the package is approximately 15pF, therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

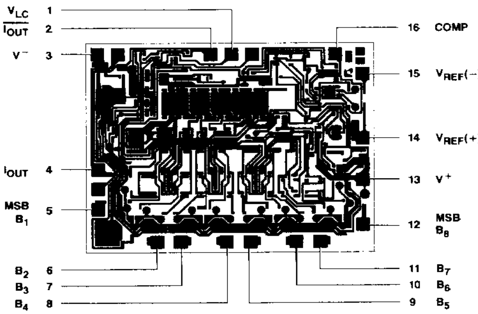
Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4μA, therefore a 1kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of Fig. 12 uses a cascode design to permit driving a 1kΩ load with less than 5pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}.

DAC-08 switching transients of "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.068" X 0.088"

ORDERING INFORMATION*

Order Number	Package Type	Temperature Range	Nonlinearity
DAC-08AQ	Ceramic DIP	−55 to +125°C	±0.1%
DAC-08Q	Ceramic DIP	−55 to +125°C	±0.19%
DAC-08AL	Leadless	−55 to +125°C	±0.1%
DAC-08L	Leadless	−55 to +125°C	±0.19%
DAC-08HQ	Ceramic DIP	0 to +70°C	±0.1%
DAC-08EQ	Ceramic DIP	0 to +70°C	±0.19%
DAC-08CQ	Ceramic DIP	0 to +70°C	±0.39%
DAC-08HL	Leadless	0 to +70°C	±0.1%
DAC-08EL	Leadless	0 to +70°C	±0.19%
DAC-08CL	Leadless	0 to +70°C	±0.39%
DAC-08HN	Plastic	0 to +70°C	±0.1%
DAC-08EN	Plastic	0 to +70°C	±0.19%
DAC-08CN	Plastic	0 to +70°C	±0.39%
DAC-08AX	Dice	−55 to +125°C	±0.1%
DAC-08X	Dice	−55 to +125°C	±0.19%
DAC-08HX	Dice	0 to +70°C	±0.1%
DAC-08EX	Dice	0 to +70°C	±0.19%
DAC-08CX	Dice	0 to +70°C	±0.39%

*Also available with burn-in processing. To order add suffix B to part number.