National Semiconductor

PRELIMINARY

DP8350 Series CRT Controllers

General Description

The DP8350 Series of CRT Controllers are single-chip bipolar (I^2L technology) circuits in a 40-pin package. They are designed to be dedicated CRT display refresh circuits. Three standard products are available, designated DP8350, DP8352, DP8353. Custom devices, however, are available in a broad range of mask programmable options.

The CRT Controller (CRTC) provides an internal dot rate crystal controlled oscillator for ease of system design. For systems where a dot rate clock is already provided, an external clock may be inputted to the CRTC. In either case system synchronization is made possible with the use of the buffered Dot Rate Clock Output.

The DP8350 Series has 11 character generation related timing outputs. These outputs are compatible for systems with or without line buffers, using character ROMs, or DM86S64-type latch/ROM/shift register circuits.

12 bits (4k) of bidirectional TRI-STATE® character memory addresses are provided by the CRTC for direct interface to character memory.

Three on-chip registers provide for external loading of the row starting address, cursor address, and top-of-page address.

A complete set of video outputs is available including cursor enable, vertical blanking, horizontal sync, and vertical sync.

The DP8350 Series CRTC provides for a wide range of programmability using internal mask programmable ROMs:

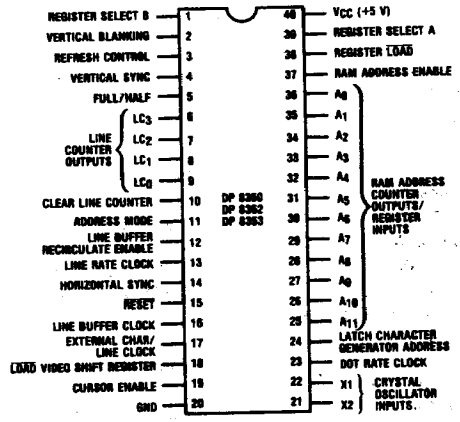
- Character Field (both number of dots/character and number of scan lines/character)
- Characters per Row
- Character Rows per Video Frame
- Format of Video Outputs

The CRTC also provides system sync and program inputs including Refresh Control, Reset, and Address Mode.

Features

- Internal crystal controlled dot rate oscillator
- External dot rate clock input
- Buffered dot rate clock output
- Timing pulses for character generation
- Character memory address outputs (12 bits)
- Internal cursor address register
- Internal row starting address register
- Internal top-of-page address register (for scrolling)
- Programmable horizontal and vertical sync outputs
- Programmable cursor enable output
- Programmable vertical blanking output
- 2 programmable refresh rates, pin selectable
- Programmable characters/row (128 max.)
- Programmable character field size (up to 16 dots x 16 scan line field size)
- Programmable scan lines/frame (512 max.)
- Programmable character rows/frame
- Single +5V power supply
- Inputs and outputs TTL compatible
- Direct interface with DM86S64 character generator
- Ease of system design/application

Connection Diagram



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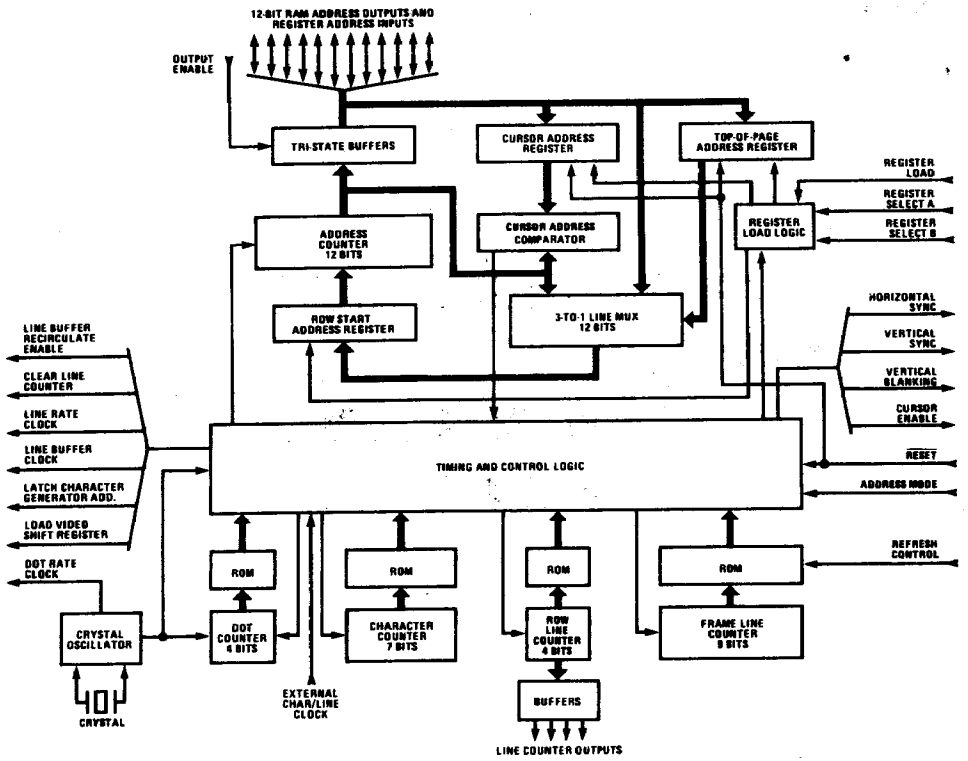
Block Diagram



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The Video Display

Discussion of the CRT Controller necessitates an understanding of the video display as presented by a raster scan monitor. The resolution of the data displayed on the monitor screen is a function of the dot size. As shown in *Figure 1*, the dot size is determined by the frequency of the system dot clock. The visible size of the dot can be modified to less than 100% by external gating of the serial video data. The CRT Controller organizes the dots into cell groupings that define video rows. These cells are accessed by a specific horizontal address output (4096 maximum) and are resolved by a row scan-line-counter output (16 maximum) as shown in *Figure 2*. The relation of the video portion of a frame to the horizontal blanking and vertical blanking intervals is shown in *Figure 3* in a two-dimensional format.

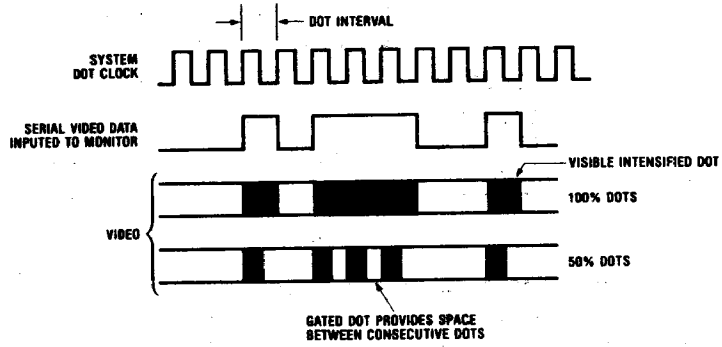

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FIGURE 1. Dot Definition

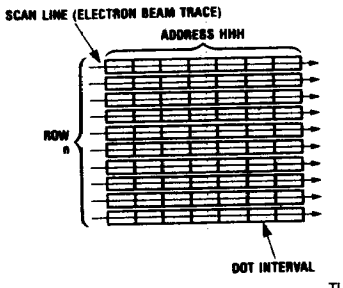

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FIGURE 2. Character Cell Definition (Example Shown Is a 7 x 10 Character Cell)

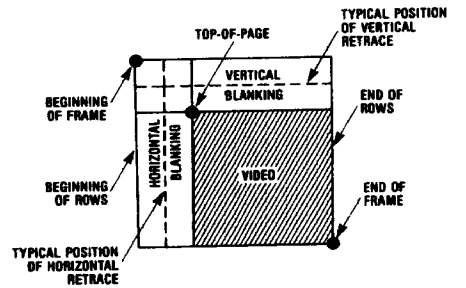

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FIGURE 3. Frame Format Definition

Character Generation/Timing Outputs

The CRT controller provides 11 interface timing outputs for line buffers, character generator ROMs, DM86S64-type latch/ROM/shift register combination character generators, and system status timing. All outputs are buffered to provide TTL compatible direct interface to popular system circuits such as:

- DM86S64 Series Character Generators
- MM52116 Series Character ROMs
- DM74166 Dot Shift Register
- MM5034, MM5035 Octal 80-Bit Shift Registers (Line Buffers)

Dot Rate Clock: This output is provided for use in system synchronization and interface to the dot shift register used in character generation. This output is non-inverting with respect to an external clock applied to the X1 oscillator input (see *Figure 6*). The dot rate clock output exhibits a 50% duty cycle. All CRTC output logic transitions are synchronous with the rising edge of the Dot Rate Clock output.

Latch Character Generator Address (Character Rate Clock): This output provides an active clock pulse at character rate frequency which is active at all times. The rising edge of this pulse is synchronous with the beginning of each character cell. This output is intended for direct interface to character/video generation data latch registers.

Line Rate Clock: This output provides an active clock pulse at scan-line rate frequency (horizontal frequency), which is active at all times. The falling edge of this pulse is synchronous with the beginning of horizontal blanking. This output is intended for direct interface to character generation scan line counters.

Load Video Shift Register: This output provides a character rate signal intended for direct interface to the video dot shift register used in character generation. Active low pulses are outputted only during video time. As a result of the inactive time, horizontal and vertical video blanking can be derived from this output signal.

Clear Line Counter: This output signal is active only during the first scan line of all rows.It exhibits an active low pulse identical and synchronous to the Line Rate Clock and is provided for direct interface to character generation scan line counters.

Line Counter Outputs (LC_0 to LC_3): These outputs clock at line rate frequency, synchronous with the falling edge of the line rate clock, and provide a consecutive binary count for each scan line within a row. These outputs are provided for system designs that require decoded information indicating the present scan line position within a row. These outputs are always active, however, the next to the last row during vertical blanking will exhibit an invalid line count as a function of internal frame synchronization.

Line Buffer Clock: This output directly interfaces to data shift registers when they are incorporated as line buffers in a system design (see *Figure 16*). This signal is active at character rate frequency and is intended for shift registers that shift on a falling edge clock. This output is inactive during all horizontal blanking intervals yielding the number of active clocks per scan line equal to the number of video characters per row. For custom requirements, the duty cycle of this output is mask programmable.

Line Buffer Recirculate Enable: This output is provided to control the input loading mode of the data shift register (line buffer) when used in a system design. The format of this output is intended for shift registers that load external data into the input with the mode control in the low state, and load output data into the input (recirculate) with the mode control in the high state. This output will transition to the low state, synchronous with the line rate clock falling edge, for one complete scan line of each row. The position of this scan line will either be the first scan line of the addressed row, or the last scan line of the previous row depending upon the logic level of the address mode input (pin 11), tabulated in Table III.

Memory Address Outputs/Inputs and Registers

Address Outputs (A_0-A_{11}): These 12 address bits (4k) are bi-directional TRI-STATE outputs that directly interface to the system RAM memory address bus.

In the output mode (enabled), these outputs will exhibit a specific 12-bit address for each video character cell to be displayed on the CRT screen. This 12-bit address increments sequentially at character rate frequency and is valid at the address bus 2 character times prior to the addressed character appearing as video on the CRT screen. This pipelining by 2 characters is provided to allow sufficient time for first, accessing the RAM memory, and second, accessing the character generation memory with the RAM memory data. Since a character cell is comprised of several scan lines of the CRT beam, the sequential address output string for a given video row is identically repeated for each scan line within the row. The starting address for each video scan line is stored within an internal 12-bit register called the Row Start Register. At the beginning of each video scan line, the internal address counter logic is preset with the contents of the Row Start Register (see *Figure 4*). To accomplish row by row sequential addressing, internal logic updates the Row Start Register at the beginning of the first scan line of a video row with the last address + 1 of the last scan line of the previous video row. Since the number of address locations on the video screen display is typically much less than the 4k dimension of the 12-bit address bus, an internal 12-bit register called the Top Of Page Register, contains the starting address of the first video row. Internal logic loads the contents of this top of page register into the Row Start Register at the beginning of the first scan line of the first video row. The Top Of Page Register is loaded with address zero whenever the Reset input is pulsed to the logic "0" state.

In the input mode (disabled), external addresses can be loaded into the internal 12-bit registers by external control of the register select A, register select B, and register $\overline{\text{load}}$ inputs (see Table I). As a result of specific external loading of the contents of the Row Start Register, Top Of Page Register, and the Cursor Register, row by row page scrolling, non-sequential row control, and cursor location control, can easily be accomplished.

During the non-video intervals, the address output operation is modified. During all horizontal blanking intervals, the incrementing of the address counter is inhibited and the address count is held constant at the last video address + 1. For example, if a video row has an 80 character cell format and addressing for the video portion of a given scan line

Memory Address Outputs/Inputs and Registers (Continued)

starts at address 1, the address counter will increment up through address 81. Address 81 is held constant during the horizontal blanking interval until 3 character times before the next video scan line. At this point, the address counter is internally loaded with the contents of the Row Start Register which may contain address 1 or 81 as a function of internal control, or a new address that was loaded from the external bus. During vertical blanking, however, this loading of the internal address counter with the contents of the Row Start Register is inhibited providing scan line by scan line sequential address incrementing. This allows minimum access time to the CRTC when the address counter outputs are being used for dynamic RAM refresh.

RAM Address Enable Input: At all times the status of the bi-directional address outputs is controlled externally by the logic level of the enable input. A 'low' logic level at this input places the address outputs in the TRI-STATE (disabled) input mode. A 'high' logic level at this input places the address outputs in the active (enabled) output mode.

Register $\overline{\text{Load}}$/Select Inputs: When the Register $\overline{\text{Load}}$ input is pulsed to the logic 'low' state, the Top Of Page, Row Start, or Cursor Register will be loaded with a 12-bit address which originates from either the internal address counter or the external address bus (refer to discussion on register loading constraints). The destination register is selected prior to the load pulse by setting the register select inputs to the appropriate state as defined in Table I.

TABLE I. Register Load Truth Table

Register Select A (Pin 39)	Register Select B (Pin 1)	Register Load Input (Pin 38)	Register Loading Destination
0	0	0	No Select
0	1	0	Top-of-Page
1	0	0	Row-Start*
1	1	0	Cursor
X	X	1	No Load

*During the vertical blanking interval, a load to this register is internally routed to the Top-Of-Page register.

Internal Registers and Loading Constraints: There are 3 internal 12-bit registers that facilitate video screen management with respect to row-by-row page scrolling, non-sequential row control and cursor location. These registers can be loaded with addresses from the external address bus while the address outputs are disabled (RAM address enable input in the low state), by controlling the register select and load inputs within the constraints of each register.

The Row-Start Register (RSR) holds the starting address for each scan line of the video portion of a frame. The video addressing format is completely determined by the contents of this register. With no external loading, the RSR is automatically loaded by internal control such that row-by-row sequential addressing is achieved. Referring to *Figure 4*, the RSR is loaded automatically once for each video row during the first addressed scan line. The source of the loaded address is internally controlled such that the RSR load for the first video row comes from the Top-Of-Page Register. The RSR load for all subsequent video rows comes from the address counter which holds the last displayed address + 1. If non-sequential row formatting is desired, the RSR can be loaded externally with a 12-bit address. However, this external load must be made prior to the internal automatic load. Generally speaking, the external load to the RSR should be made during the video domain of the last addressed scan line of the previous row. *Figure 4* indicates the internal automatic loading intervals which must be avoided, if the load must be made during the horizontal blanking interval. Once an external address has been loaded to the RSR, the next occurring internal automatic RSR load will be inhibited by internal detection logic. If an external load is made to the RSR during the vertical blanking interval the 12-bit address is loaded into the Top-Of-Page Register instead of the RSR as a result of internal control. This internal function is performed due to the fact that the address loaded into the RSR for the first video row can only come from the Top-Of-Page Register.

The Top-Of-Page register (TOPR) holds the address of the first character of the first video row. As a function of internal control the contents of this register are loaded into the RSR at the beginning of the first addressed scan line of the first video row (see *Figure 4*). This loading operation is strictly a function of internal control and cannot be overridden by an external load to the RSR. For this reason, any external load to the RSR during the vertical blanking interval is interpreted internally as TOPR load. When the Reset input is pulsed to the logic "0" state, the TOPR register is loaded with address zero by internal control. This yields a video page display with the first row of sequential addressing beginning at zero. Page scrolling can be accomplished by externally loading a new address into the TOPR. This loading operation can be performed at any time during the frame prior to the interval where the TOPR is loaded automatically into the RSR (see *Figure 4*). Once the TOPR has been loaded, it does not have to be accessed again until the contents are to be modified.

The Cursor Register (CR) holds the present address of the cursor location. A true comparison of the address counter outputs and the contents of the CR results in a Cursor Enable output signal delayed by two character times. When the $\overline{\text{Reset}}$ input is pulsed to the logic "0" state, the contents of the CR are set to address zero by internal control. Modifying the contents of the CR is accomplished by external loading at any time during this frame. Typically, loading is performed only during intervals when the address outputs are not actively controlling the video display. Once the CR has been loaded, it does not have to be accessed again until the contents are to be modified.

Video-Related Outputs

Horizontal Sync: This output provides the necessary scan line rate sync signal for direct interface to either three-terminal or composite sync monitors. The pulse width, position, and logic polarity are mask programmable, in character time increments, for custom requirements. This output may also be mask programmed to have RS-170 compatible serration pulses during the vertical sync interval (refer to DP8352 format and *Figure 15*).

Video-Related Outputs (Continued)

Vertical Sync: This output provides the necessary frame rate sync signal for direct interface to either three-terminal or composite sync monitors. The pulse width, position, and logic polarity are mask programmable, in scan line increments, for custom requirements.

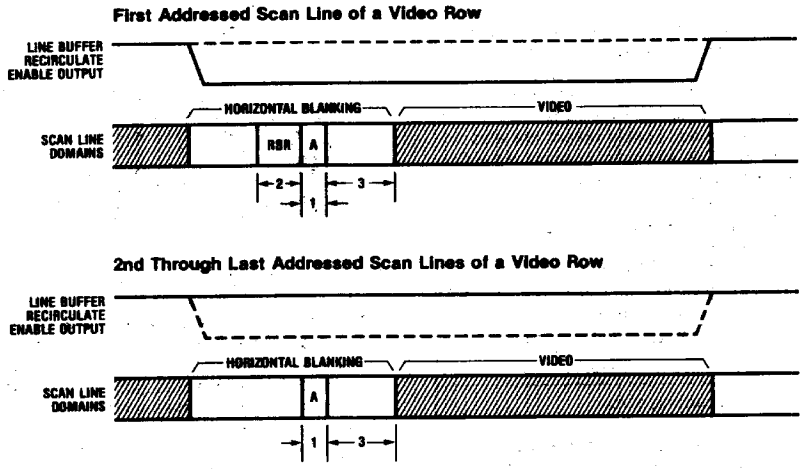
Cursor Enable: This output provides a signal that is intended to be combined with the video signal to display a cursor attribute which serves as a visual pointer for video RAM location. Internally, the 12-bit address count is continuously being compared with the 12-bit address stored in the Cursor Register. When a true compare is detected, an active high level signal will be present at the Cursor Enable output, delayed by 2 character times after the corresponding address bus output. The signal is delayed by 2 character times so that it will be coincident with the video information resulting from the corresponding address. Mask programmability allows the cursor enable output signal to be formatted such that a signal will be outputted for all addressed scan lines of a video character cell or any single scan line of that cell. The cursor enable output signal is inhibited during the horizontal and vertical blanking intervals so that video blanking is maintained. When the addressing is advanced by setting the address mode input (pin 11) in the logic "0" state, the cursor enable signal will also be shifted with respect to the scan line count. Specifically, for a character cell with the cursor output active on all addressed scan lines of the cell, the first scan line of the cursor signal will occur at the last scan line count of the previous video row, and the last scan line count of the addressed character cell will have no cursor output signal. This mode of operation gives rise to a unique situation for the first video row where the first addressed scan line of a character cell has no cursor output signal since its advanced scan line position is inhibited by the vertical blanking interval.

CRT System Control Functions

Refresh Control Input: This input provides a logic level selectable CRT system refresh rate. Typically, this input will select either a 60 Hz or 50 Hz refresh rate to provide geographical marketing flexibility. However, mask programmability provides the capability of a wide range of frequencies for custom requirements. For definition of the input logic truth table and the refresh rate format, refer to Table II and the standard device type format tables.

Table II. Refresh Rate Select Truth Table

Refresh Control (Pin 3) Logic Level	Frame Refresh Rate			
	Symbol	DP8350	DP8352	DP8353
1	f1	60 Hz	60 Hz	60 Hz
0	f0	50 Hz	50 Hz	50 Hz



Note 1: Dimensions are in character time intervals.

Note 2: "A" denotes the interval that the address counter is preset with the contents of the Row Start Register.

Note 3: "RSR" denotes the interval that the Row Start Register is internally loaded with either the contents of the Top-Of-Page Register (1st video row) or the last video address + 1 from the address counter.

FIGURE 4. Automatic Internal Loading Intervals

CRT System Control Functions (Continued)

Vertical Blanking Output: This output provides a signal that transitions at the end of the last video scan line of the last video row and indicates the beginning of the vertical blanking interval. This signal transitions back to the inactive state during the row of scan lines just prior to the first video row. The transition position within this last row of vertical blanking, as well as the active logic polarity, is a function of the particular device format (item 21 of the format tables) or is mask programmable for custom requirements.

Address Mode: When a system utilizes a line buffer shift register, the scan line of addressing for a row is used to load the shift register. As a result of this loading operation, addressing for a particular row will not begin accessing the video RAM until the second scan line of addressing for the row. It also follows that the first scan line of a row can only exhibit addressed data for the previous video row that is in the shift register. This offset in addressing becomes a problem for character generation designs that output video on the first scan line of a row (with respect to the line counter outputs). The result is invalid data being displayed for the first scan line. One solution would be to utilize a character generation design that began outputting video on the second scan line of a row. However, since most single chip character generators begin video on the first scan line, the DP8350 series CRT controller provides a pin selectable advanced addressing mode which will compensate for addressing shifts resulting from shift register loading. Referring to Table III, a high logic level at this input will cause addressing to be coincident with the scan line counter positions of a row, and a low logic level at this input will cause addressing to start on the last scan line counter position of the previous row. This shifted alignment of the addressing, with respect to the designated scan lines of a row, is diagrammed in *Figure 5*. Characteristically, it follows that, when addressing is advanced by one scan line, the Line Buffer Recirculate Enable output and the Cursor Enable output are also advanced by one scan line. This advanced position of the Cursor Enable output may deserve special consideration depending upon the system design.

Table III. Address Mode Truth Table

Address Mode Input (Pin 11) (Logic Level)	New Row Addressing At Address Outputs and Line Buffer Recirculate Enable Logic Low Level (Scan Line Position)
0	Last scan line of previous row
1	First scan line of row

Full/Half Row Control: This control input is provided for applications that require the option of half-page addressing. As an example, if the normal video page format is 80 characters/row by 24 rows, setting this input to the logic "0" state will cause the video format to become evenly spaced at 80 characters/row by 12 rows. Specifically, when this input is in the logic "0" state, row addressing is repeated for every other row. This yields successive groups of two rows of identical addressing. The second row of addressing, however, has the Load Video Shift Register output and the Cursor Enable output internally inhibited to provide the necessary video blanking. Setting this input to the logic "1" state yields normal frame addressing.

External Character/Line Rate Clock: This input is intended to aid testing of the CRTC and is not meant to be used as an active input in a CRT system. When this input is left open, it is guaranteed not to interfere with normal operation.

Reset Input: This input is provided for power-up synchronization. When brought to the logic "0" state, device operation is halted. Internal logic is set at the beginning of vertical blanking, and the Top-Of-Page Register and the Cursor Register are loaded with address zero. When this input returns to the logic "1" state, device operation resumes at the vertical blanking interval followed by video addressing which begins at zero. This input has hysteresis and may be connected through a resistor to V_{CC} and through a capacitor to ground to accomplish a power-up Reset. The logic "0" state should be maintained for a minimum of 250 ns.

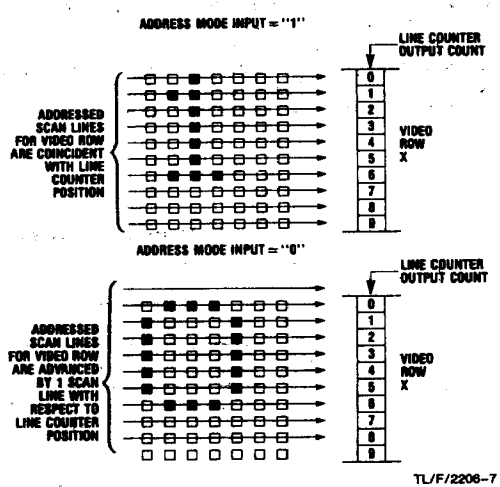


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FIGURE 5. Address Mode Functionality

Crystal Inputs X1 and X2: The "Pierce"-type oscillator is controlled by an external crystal providing parallel resonant operation. Connection of external bias components is made to pin 22 (X1) and pin 21 (X2) as shown in *Figure 6*. It is important that the crystal be mounted in close proximity to the X1 and X2 pins to ensure that printed circuit trace lengths are kept to an absolute minimum. Typical specifications for the crystal are shown in Table IV for each of the standard products, DP8350, DP8352, and DP8353. When customer mask options require higher frequencies, it may be necessary to change the crystal specifications and biasing components. If the CRTC is to be clocked by an external system dot clock, pin 22 (X1) should be driven directly by Schottky family logic while pin 21 (X2) is left open. The typical threshold for pin 22 (X1) is $V_{CC}/2$.

CRT System Control Functions (Continued)

Table IV. Typical Crystal Specifications

Parameter	Specification		
	DP8350	DP8352	DP8353
Type	At-Cut		
Frequency	10.92 MHz	7.02 MHz	17.6256 MHz
Tolerance	0.005% at 25°C		
Stability	0.01% from 0°C to +70°C		
Resonance	Fundamental, Parallel		
Maximum Series Resistance	50Ω		
Load Capacitance	20 pF		

Custom Order Mask Programmability: The DP8350 Series CRT controller is available in three standard options designated DP8350, DP8352, and DP8353. The functional format of these devices was selected to meet the typical needs of CRT terminal designs. In order to accommodate specific customer formats, the DP8350 series CRT controller is mask programmable with a diverse range of options available. The items listed in the program table worksheet indicate the available options, while Table V tabulates the programming constraints.

Table V. Mask Programming Limitations

Designation	Parameter		Min Value	Max Value
f_{DOT}	Dot Rate Frequency		DC	30 MHz
f_{CHAR}	Character Rate Frequency		DC	2.5 MHz
—	Line Buffer Clock Logic "0" Width (Item 20 × Item 24)		200 ns	
Item 3	Dots per Character Field Width		4	16
Item 4	Scan Lines per Character Field		2	16
Item 12	Scan Lines per Frame			512
Item 14	Character Times per Row	Video	5	122
		Blanking	6	123
Item 11	Scan Lines per Vertical Blanking		(Item 4) +2	
If the cursor enable output, Item 22, is active on only one line of a character row, then Item 21 value must be either "1" or "0" or equivalent to the line selected for the cursor enable output.				

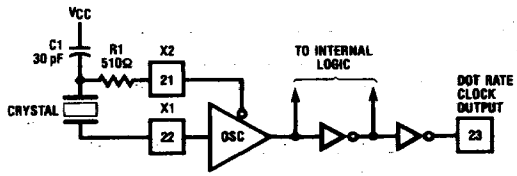

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FIGURE 6. Dot Clock Oscillator Configuration with Typical External Bias Circuitry Shown

DP8350 Series Custom Order Format Table

This table is provided as a worksheet to aid in determining the programmed configuration for custom mask options. Refer to Table V for a list of programming limitations.

Item No.	Parameter		Value	
1	Character Font Size (Reference Only)	Dots per Character (Width)		
2		Scan Lines per Character (Height)		
3	Character Field Block Size	Dots per Character (Width)		
4		Scan Line per Character (Height)		
5	Number of Video Characters per Row			
6	Number of Video Character Rows per Frame			
7	Number of Video Scan Lines (Item 4 x Item 6)			
8	Frame Refresh Rate (Hz) (two pin selectable frequencies allowed) (Item 13 ÷ Item 12)		f1 =	f0 =
9	Delay after Vertical Blank start to start of Vertical Sync (Number of Scan Lines)			
10	Vertical Sync Width (Number of Scan Lines)			
11	Interval between Vertical Blank start and start of Video (Number of Scan Lines of Video Blanking)			
12	Total Scan Lines per Frame (Item 7 + Item 11)			
13	Horizontal Scan Frequency (Line Rate) (kHz) (Item 8 x Item 12)			
14	Number of Character Times per Scan Line			
15	Character Clock Rate (MHz) (Item 13 x Item 14)			
16	Character Time (ns) (1 ÷ Item 15)			
17	Delay after Horizontal Blank start to Horizontal Sync start (Character Times)			
18	Horizontal Sync Width (Character Times)			
19	Dot Frequency (MHz) (Item 3 x Item 15)			
20	Dot Time (ns) (1 ÷ Item 19)			
21	Vertical Blanking Output Stop before start of Video (Number of Scan Lines) (Range = Item 4 − 1 line to 0 lines)			
22	Cursor Enable on all Scan Lines of a Row? (Yes or No) If not, which Line?			
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)			
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments) (Typically ½ Item 3 rounded up)			
25	Serration Pulse Width, if used (Character Times) (See *Figure 13*)			
26	Horizontal Sync Pulse Active state logic level (1 or 0)			
27	Vertical Sync Pulse Active state logic level (1 or 0)			
28	Vertical Blanking Pulse Active state logic level (1 or 0)			

Video Monitor: Manufacturer and Model No. (For Engineering Reference)

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temp. (soldering, 10 seconds)	300°C

Operating Conditions (Note 6)

	Min.	Max.	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	+70	°C

Electrical Characteristics V_{CC} = 5V ± 5%, T_A = 0°C to +70°C (Notes 2, 3, and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage All Inputs Except X1, X2 $\overline{RESET}$ $\overline{RESET}$		2.0 2.6			V V
V_{IL}	Logic "0" Input Voltage All Inputs Except X1, X2				0.8	V
V_{HYS}	$\overline{RESET}$ Input Hysteresis			0.4		V
V_{clamp}	Input Clamp Voltage All Inputs Except X1, X2	I_{IN} = −12 mA		−0.8	−1.2	V
I_{IH}	Logic "1" Input Current A_0-A_{11}	Enable Input = 0V, V_{CC} = 5.25V, V_{IN} = 5.25V		10	100	μA
	All Other Inputs Except X1, X2	V_{CC} = 5.25V, V_{IN} = 5.25V		2.0	20	μA
I_{IL}	Logic "0" Input Current A_0-A_{11}	Enable Input = 0V, V_{CC} = 5.25V, V_{IN} = 0.5V		−20	−100	μA
	All Other Inputs Except X1, X2	V_{CC} = 5.25V, V_{IN} = 0.5V		−20	−100	μA
V_{OH}	Logic "1" Output Voltage	I_{OH} = −100 μA	3.2	4.1		V
		I_{OH} = −1 mA	2.5	3.3		V
V_{OL}	Logic "0" Output Voltage	I_{OL} = 5 mA		0.35	0.5	V
I_{OS}	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0V (Note 4)	10	40	100	mA
I_{CC}	Power Supply Current (Note 10)	V_{CC} = 5.25V		220	300	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min./max. limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for T_A = 25°C and V_{CC} = 5.0V and are intended for reference only.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max. or min. are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Electrical specifications do not apply to pin 17, external char/line clock, as this pin is used for production testing only.

Note 6: Functional operation of device is not guaranteed when operated beyond specified operating condition limits.

Switching Characteristics V_{CC} = 5.0V ± 5%, T_A = 25°C (Note 7)

Symbol	Parameter	Load Circuit	Notes	Min	Typ	Max	Units
Symmetry	Dot Rate Clock Output High Symmetry With Crystal Control	1		50% − 4	50% − 2	50% + 1	ns
t_{pd1}	XI Input to Dot Rate Clock Output Positive Edge	1			17	22	ns
t_{pd0}	XI Input to Dot Rate Clock Output Negative Edge	1			21	26	ns
t_{D1}	Dot Clock to Load Video Shift Register Negative Edge	1			6.0	10	ns
t_{D2}	Dot Clock to Load Video Shift Register Positive Edge	1			11	15	ns
t_{D3}	Dot Clock to Latch Character Generator Positive Edge	1			8.0	13	ns
t_{D4}	Dot Clock to Latch Character Generator Negative Edge	1			6.0	10	ns
t_{D2}-t_{D3}	Latch Character Generator Positive Edge to Load Video Shift Register Positive Edge	1		0	3.0		ns
t_{D5}	Dot Clock to Line Buffer Clock Negative Edge	1			23	35	ns
t_{PW1}	Line Buffer Clock Pulse Width	1	8,9	N(DT)	N(DT) + 8	N(DT) + 12	ns
t_{D6}	Dot Clock to Cursor Enable Output Transition	1			24	36	ns
t_{D7}	Dot Clock to Valid Address Output	1			15	25	ns
t_{D8_0}	Latch Character Generator to Line Rate Clock Neg. Transition	1	8,10		425 + DT	500 + DT	ns
t_{D8_1}	Latch Character Generator to Line Rate Clock Pos. Transition	1	8,10		300 + DT	400 + DT	ns
t_{D9_0}	Latch Character Generator to Clear Line Counter Neg. Transition	1	8,10		525 + DT	700 + DT	ns
t_{D9_1}	Latch Character Generator to Clear Line Counter Pos. Transition	1	8,10		290 + DT	400 + DT	ns
t_{D8_1}-t_{D9_1}	Clear Line Counter Pos. Transition to Line Rate Clock Pos. Transition	1	10		10	60	ns
t_{D10}	Line Rate Clock to Line Counter Output Transition	1			60	120	ns
t_{D11}	Line Rate Clock to Line Buffer Recirculate Enable Transition	1			195	300	ns
t_{D12}	Line Rate Clock to Vertical Blanking Transition	1			160	300	ns
t_{D13}	Line Rate Clock to Vertical Sync Transition	1			220	300	ns
t_{D14}	Latch Character Generator to Horizontal Sync Transition	1			96	150	ns

Switching Characteristics V_{CC} = 5.0V ±5%, T_A = 25°C (Note 7) (Continued)

Symbol	Parameter	Load Circuit	Notes	Min	Typ	Max	Units
t_{S1}	Register Select Set-up Before Register Load Negative Edge			0			ns
t_{H1}	Register Select Hold After Register Load Positive Edge			0			ns
t_{S2}	Valid Address Input Set-Up Before Register Load Positive Edge			250			ns
t_{H2}	Valid Address Hold Time After Register Load Positive Edge			0			ns
t_{PW2}	Register Load Required Pulse Width			150	65		ns
t_{LZ}, t_{HZ}	Delay from Enable Input to Address Output High Impedance State from Logic "0" and Logic "1"	2			15	30	ns
t_{ZL}, t_{ZH}	Delay from Enable Input to Logic "0" and Logic "1" from Address Output High Impedance State	2			17	30	ns

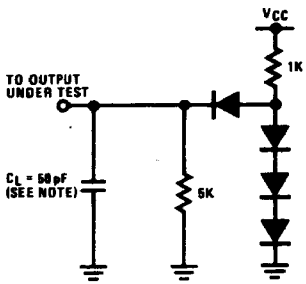
Note 7: Typical values are for V_{CC} = 5.0V and T_A = 25°C and are meant for reference only.

Note 8: "DT" denotes dot rate clock period time, item 20 from option format table.

Note 9: "N" denotes value of item 24 from option format table.

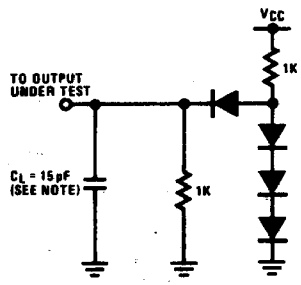
Note 10: Revised since last issue.

Switching Load Circuits



TL/F/2206–9

Load Circuit 1



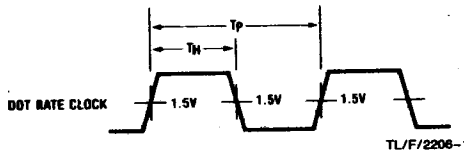
TL/F/2206–10

Load Circuit 2

Note: C_L includes probe and jig capacitance. All diodes are 1N914 or equivalent.

Switching Waveforms

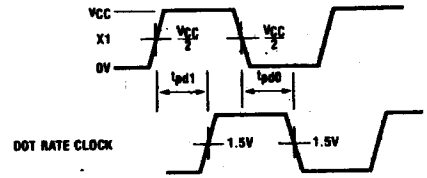
SYMMETRY = $\frac{T_H}{T_P} \times 100\%$



TL/F/2206–11

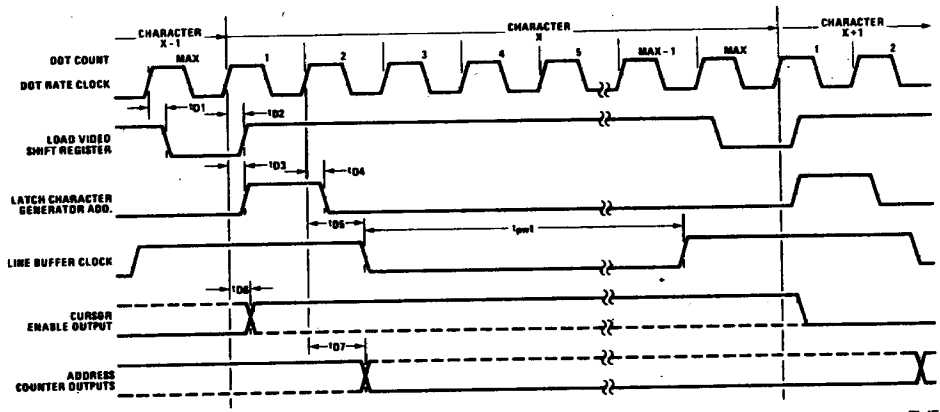
FIGURE 7. Dot Rate Clock Output Waveform Symmetry with Crystal Control

$[t_r = t_f \leq 10\ ns$
$X2\ (PIN\ 21) = OPEN]$



TL/F/2206–12

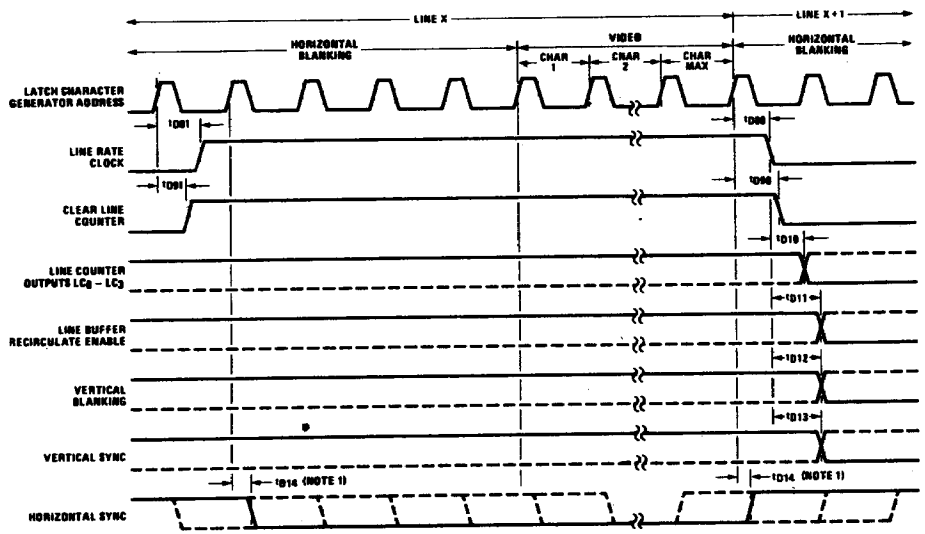
FIGURE 8. X1 Input to Dot Rate Clock Output Propagation Delay



TL/F/2206–13

Note 1: All measurement points are 1.5V

FIGURE 9. Dot/Character Rate Timing



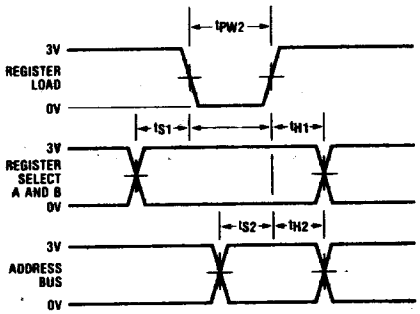
TL/F/2206–14

Note 1: Actual polarity and position of the horizontal sync start and stop points is a function of the particular device format.

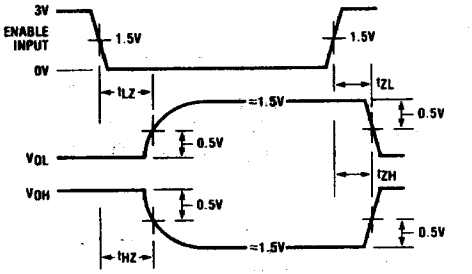
Note 2: All measurement points are 1.5V.

FIGURE 10. Character/Line Rate Timing

Switching Waveforms (Continued)



TL/F/2206–15



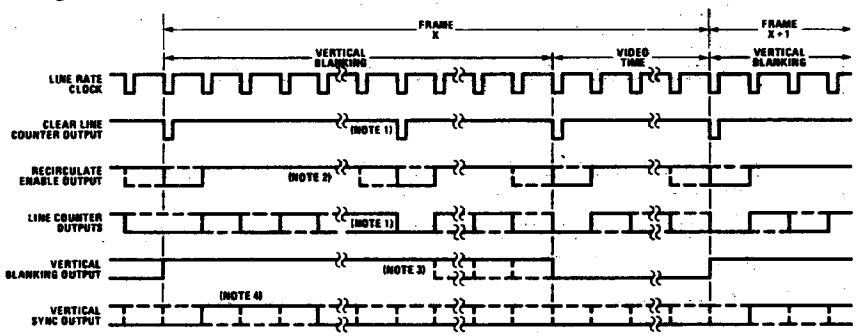
TL/F/2206–16

FIGURE 12. Address Output Enable/Disable Waveforms

Note 1: All measurement points are 1.5V.
Note 2: $t_r = t_f \leq 10$ ns.
Note 3: Address enable (pin 37) = 0V.

FIGURE 11. Register Select and Load Waveforms

Timing Diagrams



TL/F/2206–17

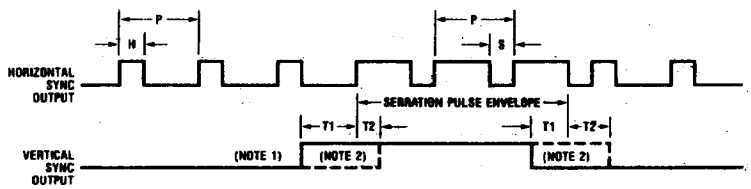
Note 1: One full row before start of video the line counter is set to zero state—this provides line counter synchronization in cases where the number of lines in vertical blanking are not even multiples of the number of lines per row.

Note 2: The position of the line buffer recirculate enable logic low level is a function of the logic level of the address mode input (see Table III).

Note 3: The stop point of the vertical blanking output active signal is a function of device type or custom option, and will always be within one row prior to video.

Note 4: The transition start and stop points of the vertical sync output signal are a function of device type or custom option.

FIGURE 14. Line/Frame Rate Functional Diagram



TL/F/2206–18

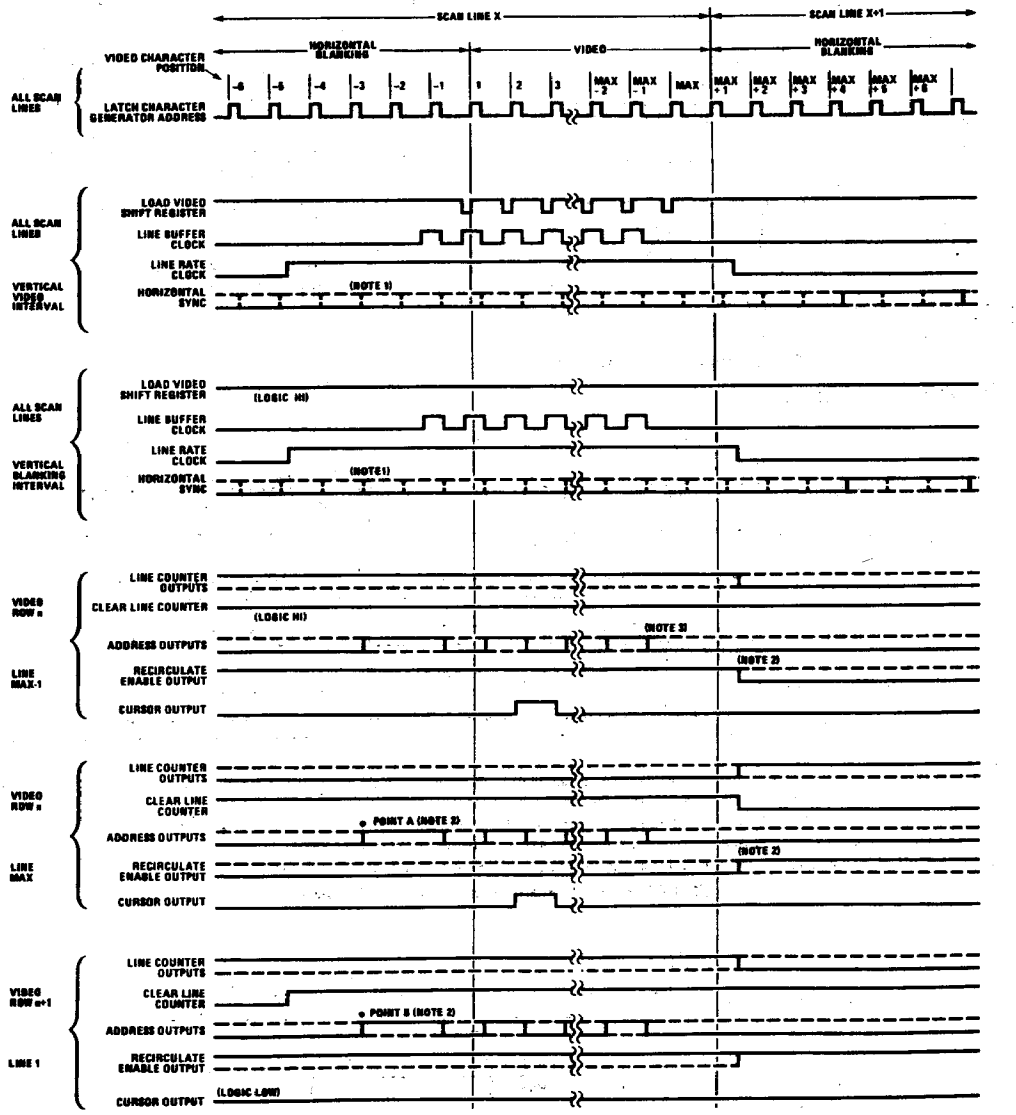
P = HORIZONTAL SCAN TIME PERIOD (ITEM 14 FROM PROGRAM TABLE)
H = HORIZONTAL SYNC WIDTH (ITEM 18 FROM PROGRAM TABLE)
S = SERRATION PULSE WIDTH (ITEM 25 FROM PROGRAM TABLE)
T1 = P-H (MAX)
T2 = H-1 CHARACTER TIME (MAX)

Note 1: The vertical sync transition point is always coincident with the beginning of horizontal blanking.

Note 2: T1 and T2 intervals represent the range of alignment offset between the vertical sync pulse and the serration pulse envelope and is a function of the horizontal sync position with respect to the beginning of horizontal blanking.

FIGURE 15. Serration Pulse Format

Timing Diagrams (Continued)



TL/F/2206–19

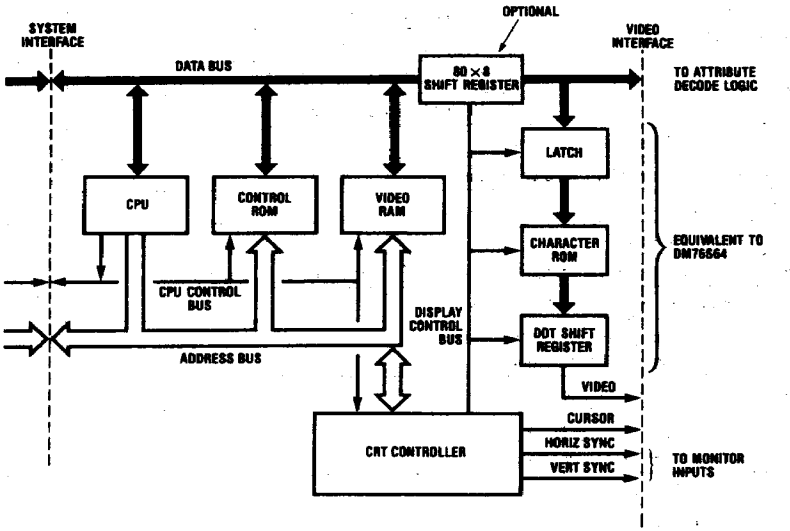
Note 1: The horizontal sync output start and stop point positions are a function of device type or custom option.

Note 2: The position of the recirculate enable output logic "0" level is dependent on the state of the address mode input. When address mode = "0", recirculate enable occurs on the max. line of a character row (solid line) and the address counter outputs all over to the new row address at point A. When address mode = "1", recirculate enable occurs on the first line of a character row (dashed line) and the address counter outputs roll over to the new row address at point B.

Note 3: The address counter outputs clock to the address of the last character of a video row plus 1. This address is then held during the horizontal blanking interval until video minus three character times. At this point the outputs are modified to the contents of the Row Start Register (RSR).

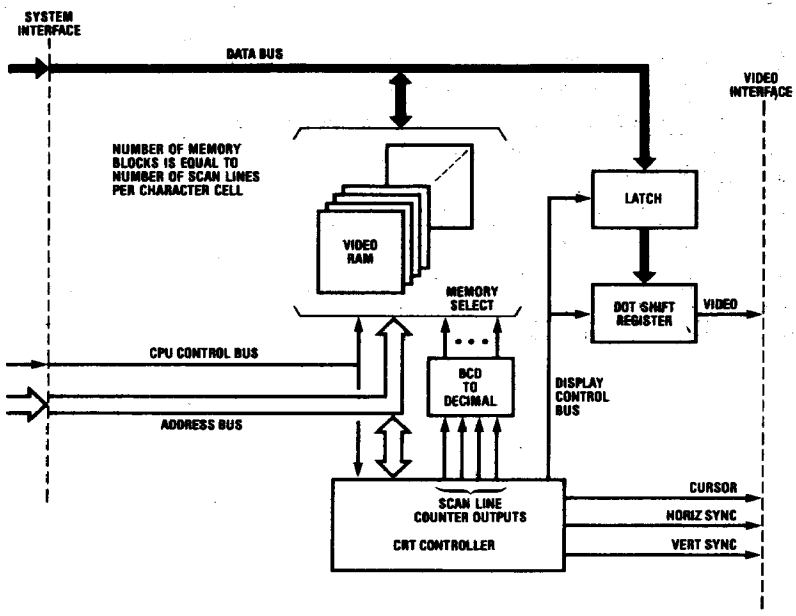
FIGURE 13. Character/Line Rate Functional Diagram

Applications



TL/F/2206–20

FIGURE 16. General System Block Diagram



TL/F/2206–21

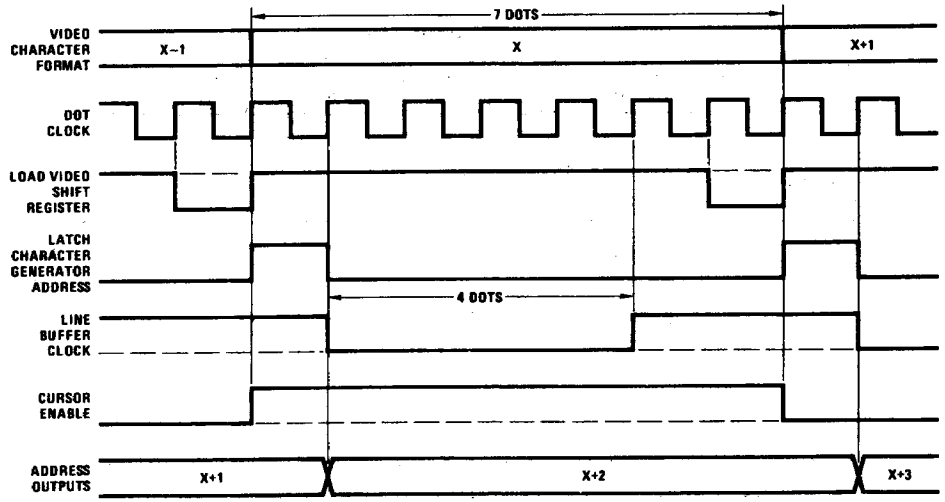
FIGURE 17. Dot-By-Dot Graphics Block Diagram

DP8350 CRT Controller

TABLE VI. Characteristic Format

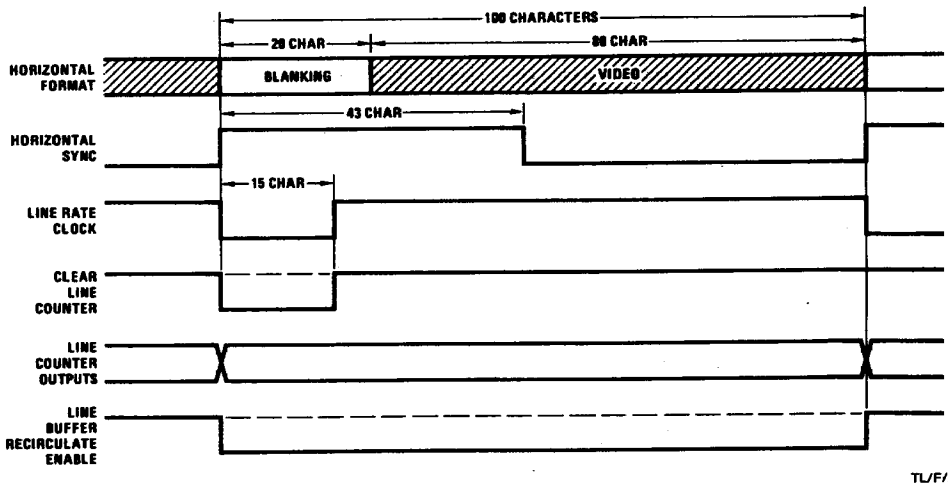
Item No.	Parameter		Value	
1	Character Font Size (Reference Only)	Dots per Character (Width)	(5)	
2		Scan Lines per Character (Height)	(7)	
3	Character Field Cell Size	Dots per Character (Width)	7	
4		Scan Lines per Character (Height)	10	
5	Number of Video Characters per Row		80	
6	Number of Video Character Rows per Frame		24	
7	Number of Video Scan Lines (Item 4 x 6 Item 6)		240	
8	Frame Refresh Rate (Hz)		f1 = 60	f0 = 50
9	Delay after Vertical Blank start to start of Vertical Sync (Number of Scan Lines)		4	30
10	Vertical Sync Width (Number of Scan Lines)		10	10
11	Interval between Vertical Blank start and start of Video (Number of Scan Lines of Video Blanking)		20	72
12	Total Scan Lines per Frame (Item 7 + Item 11)		260	312
13	Horizontal Scan Frequency (Line Rate) (Item 8 x Item 12)		15.6 kHz	
14	Number of Character Times per Scan Line		100	
15	Character Clock Rate (Item 13 x Item 14)		1.56 MHz	
16	Character Time (1 ÷ Item 15)		641 ns	
17	Delay after Horizontal Blank start to Horizontal Sync start (Character Times)		0	
18	Horizontal Sync Width (Character Times)		43	
19	Dot Frequency (Item 3 x Item 15)		10.92 MHz	
20	Dot Time (1 ÷ Item 19)		91.6 ns	
21	Vertical Blanking Output Stop before start of Video (Number of Scan Lines)		1	
22	Cursor Enable on all Scan Lines of a Row? (Yes or No)		Yes	
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)		No	
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)		4	
25	Serration Pulse Width, if used (Character Times)		—	
26	Horizontal Sync Pulse Active state logic level (1 or 0)		1	
27	Vertical Sync Pulse Active state logic level (1 or 0)		0	
28	Vertical Blanking Pulse Active state logic level (1 or 0)		1	

Video Monitor Format: Ball Brothers TV-12, TV-120 or Equivalent.



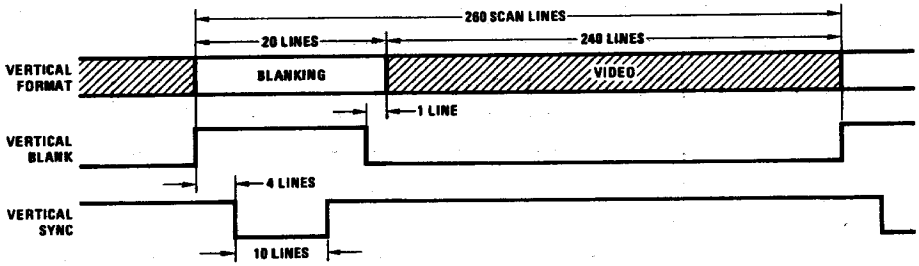
Note: Dashed lines in waveforms denote inactive state logic levels.

FIGURE 18. DP8350 Video Character Signals



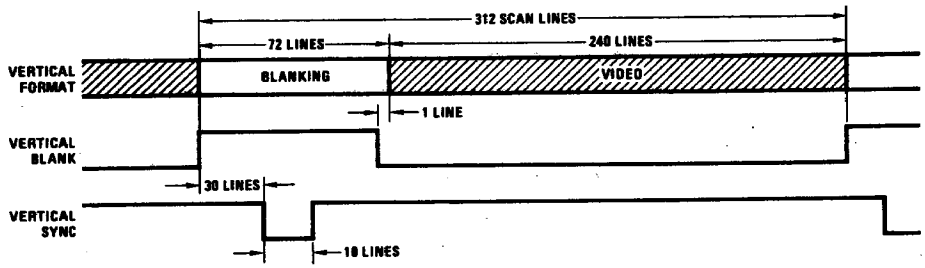
Note: Dashed lines in waveforms denote inactive state logic levels.

FIGURE 19. DP8350 Scan Line Signals



TL/F/2206–24

FIGURE 20. DP8350 60 Hz Refresh Rate Frame Signals



TL/F/2206–25

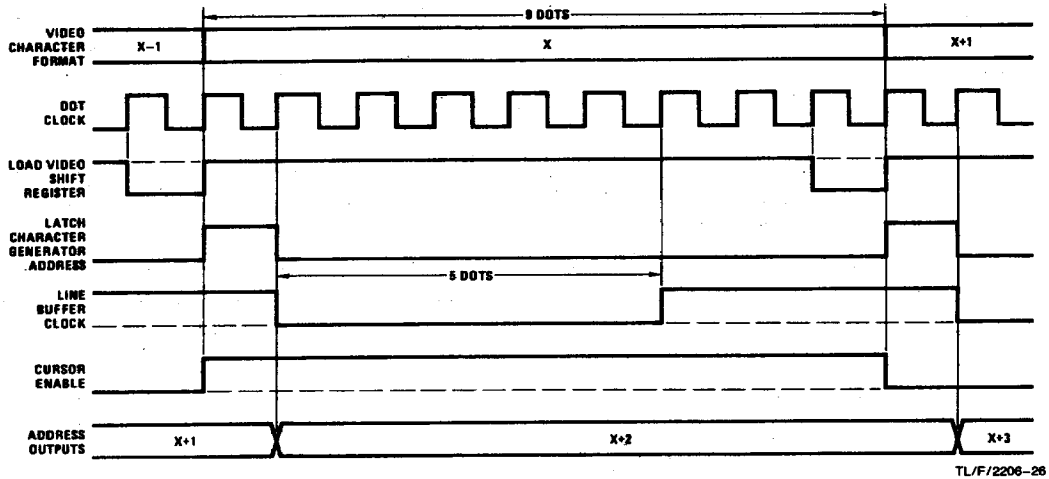
FIGURE 21. DP8350 50 Hz Refresh Rate Frame Signals

DP8352 CRT Controller

TABLE VII. Characteristic Format

Item No.	Parameter		Value	
1	Character Font Size (Reference Only)	Dots per Character (Width)	(7)	
2		Scan Lines per Character (Height)	(9)	
3	Character Field Cell Size	Dots per Character (Width)	9	
4		Scan Lines per Character (Height)	12	
5	Number of Video Characters per Row		32	
6	Number of Video Character Rows per Frame		16	
7	Number of Video Scan Lines (Item 4 x Item 6)		192	
8	Frame Refresh Rate (Hz)		f1 = 60	f0 = 50
9	Delay after Vertical Blank start to start of Vertical Sync (Number of Scan Lines)		27	53
10	Vertical Sync Width (Number of Scan Lines)		3	3
11	Interval between Vertical Blank start and start of Video (Number of Scan Lines of Video Blanking)		68	120
12	Total Scan Lines per Frame (Item 7 + Item 11)		260	312
13	Horizontal Scan Frequency (Line Rate) (Item 8 x Item 12)		15.6 kHz	
14	Number of Character Times per Scan Line		50	
15	Character Clock Rate (Item 13 x Item 14)		0.78 MHz	
16	Character Time (1 ÷ Item 15)		1282 ns	
17	Delay after Horizontal Blank start to Horizontal Sync start (Character Times)		6	
18	Horizontal Sync Width (Character Times)		4	
19	Dot Frequency (Item 3 x Item 15)		7.02 MHz	
20	Dot Time (1 ÷ Item 19)		142.4 ns	
21	Vertical Blanking Output Stop before start of Video (Number of Scan Lines)		0	
22	Cursor Enable on all Scan Lines of a Row? (Yes or No)		Yes	
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)		Yes	
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)		5	
25	Serration Pulse Width, if used (Character Times)		4	
26	Horizontal Sync Pulse Active state logic level (1 or 0)		0	
27	Vertical Sync Pulse Active state logic level (1 or 0)		0	
28	Vertical Blanking Pulse Active state logic level (1 or 0)		1	

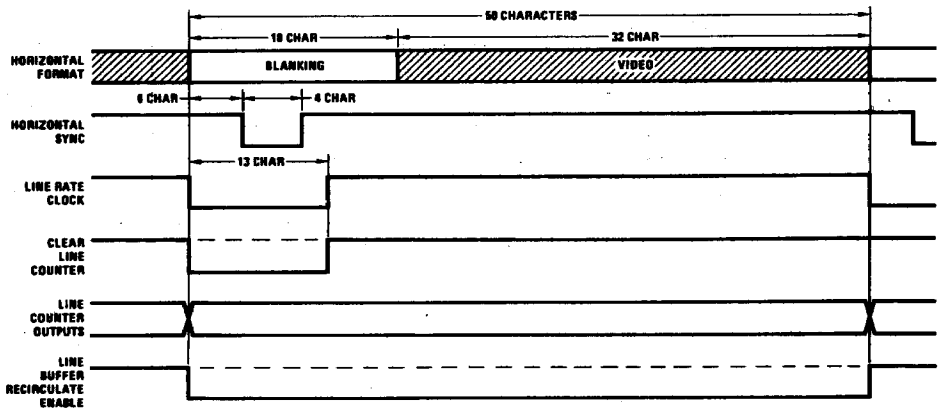
Video Monitor Format: RS-170-Compatible (Standard American TV).



TL/F/2206–26

Note: Dashed lines in waveforms denote inactive state logic levels.

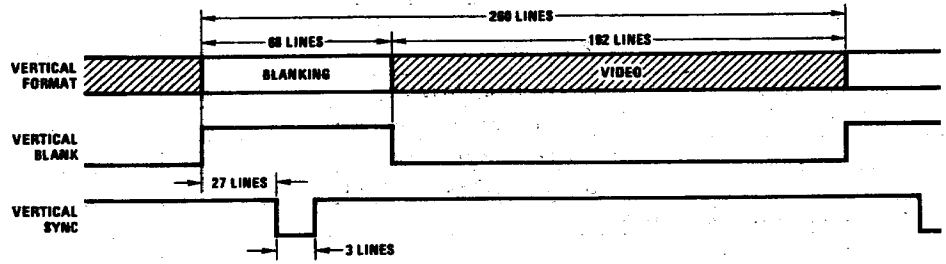
FIGURE 22. DP8352 Video Character Signals



TL/F/2206–27

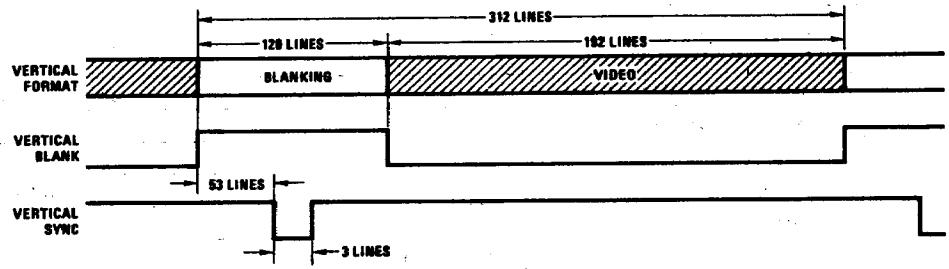
Note: Dashed lines in waveforms denote inactive state logic levels.

FIGURE 23. DP8352 Scan Line Signals



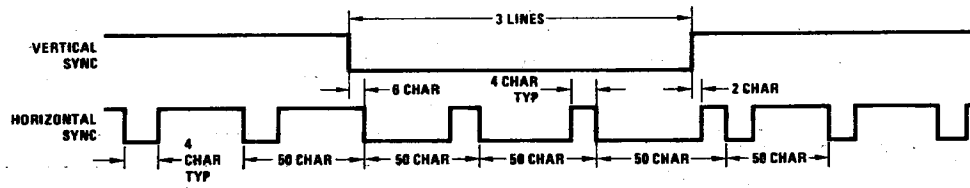
TL/F/2206–28

FIGURE 24. DP8352 60 Hz Refresh Rate Frame Signals



TL/F/2206–29

FIGURE 25. DP8352 50 Hz Refresh Rate Frame Signals



TL/F/2206–30

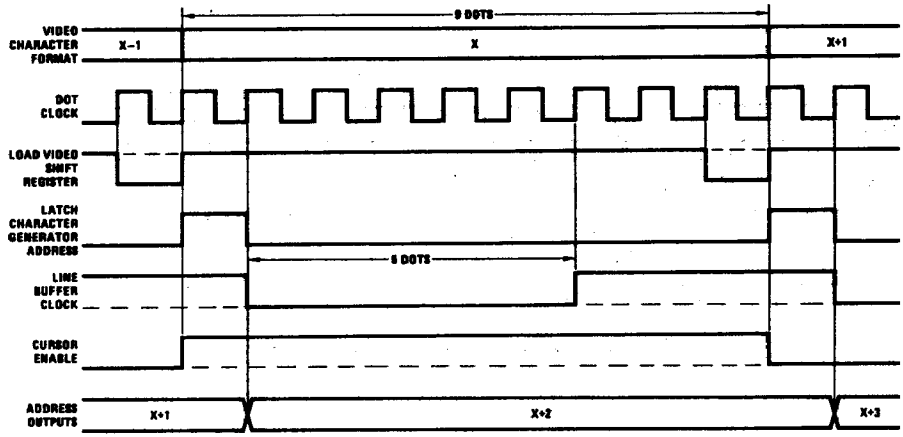
FIGURE 26. DP8352 Serration Pulse Format

DP8353 CRT Controller

TABLE VIII. Characteristic Format

Item No.	Parameter		Value	
1	Character Font Size (Reference Only)	Dots per Character (Width)	(7)	
2		Scan Lines per Character (Height)	(9)	
3	Character Field Cell Size	Dots per Character (Width)	9	
4		Scan Line per Character (Height)	12	
5	Number of Video Characters per Row		80	
6	Number of Video Character Rows per Frame		25	
7	Number of Video Scan Lines (Item 4 x Item 6)		300	
8	Frame Refresh Rate (Hz)		f1 = 60	f0 = 50
9	Delay after Vertical Blank start to start of Vertical Sync (Number of Scan Lines)		0	32
10	Vertical Sync Width (Number of Scan Lines)		3	3
11	Interval between Vertical Blank start and start of Video (Number of Scan Lines of Video Blanking)		20	84
12	Total Scan Lines per Frame (Item 7 + Item 11)		320	384
13	Horizontal Scan Frequency (Line Rate) (Item 8 x Item 12)		19.20 kHz	
14	Number of Character Times per Scan Line		102	
15	Character Clock Rate (Item 13 x Item 14)		1.9584 MHz	
16	Character Time (1 ÷ Item 15)		510.6 ns	
17	Delay after Horizontal Blank start to Horizontal Sync start (Character Times)		5	
18	Horizontal Sync Width (Character Times)		9	
19	Dot Frequency (Item 3 x Item 15)		17.6256 MHz	
20	Dot Time (1 ÷ Item 19)		56.7 ns	
21	Vertical Blanking Output Stop before start of Video (Number of Scan Lines)		1	
22	Cursor Enable on all Scan Lines of a Row? (Yes or No)		Yes	
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)		No	
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)		5	
25	Serration Pulse Width, if used (Character Times)		—	
26	Horizontal Sync Pulse Active state logic level (1 or 0)		1	
27	Vertical Sync Pulse Active state logic level (1 or 0)		1	
28	Vertical Blanking Pulse Active state logic level (1 or 0)		1	

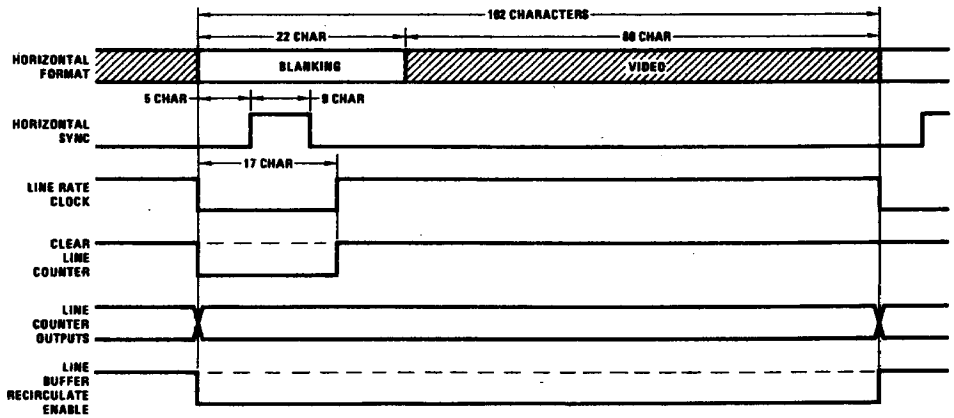
Video Monitor Format: Motorola M3003 or Equivalent.



TL/F/2206–31

Note: Dashed lines in waveforms denote inactive state logic levels.

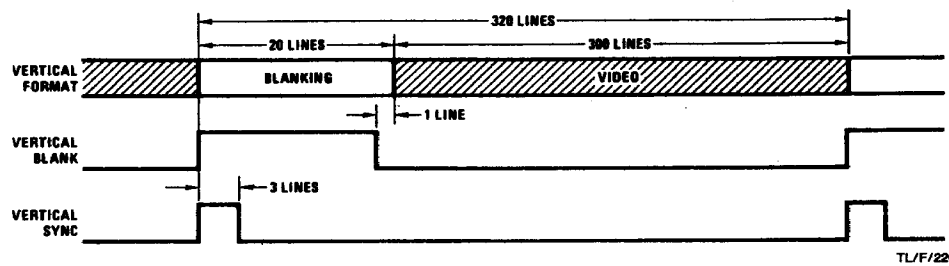
FIGURE 27. DP8353 Video Character Signals



TL/F/2206–32

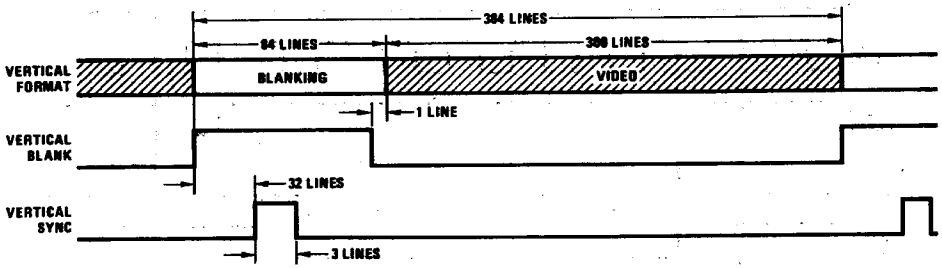
Note: Dashed lines in waveforms denote inactive state logic levels.

FIGURE 28. DP8353 Scan Line Signals



TL/F/2206–33

FIGURE 29. DP8353 60 Hz Refresh Rate Frame Signals



TL/F/2206–34

FIGURE 30. DP8353 50 Hz Refresh Rate Frame Signals