DALLAS SEMICONDUCTOR

Application Note 63
Using Nonvolatile Static RAMs

Vast resources have been expended by the semiconductor industry trying to build a nonvolatile random access read/write memory. The effort has been undertaken because nonvolatile RAM offers several advantages over other memory devices – DRAM, Static RAM, Shadow RAM, EEPROM, EPROM and ROM – which were developed to meet specific applications needs.

Characteristics of the ideal nonvolatile RAM are: low power consumption, high performance, high reliability, high density, low cost, and the ability to be used in any semiconductor memory application.

While the various memory components designed to date do not meet the ideal memory scenario, each excels in meeting one or more of the sought after attributes (Figure 1).

MEMORY ATTRIBUTES Figure 1

	COST	EASE OF INTER-FACE	NONVOLA-TILE	DENSITY	PERFOR-MANCE	READ/ WRITE	DATA RETEN-TION
DRAM	+++			+++	++	+++	
STATIC RAM		+++		+	+++	+++	
NV SRAM		+++	++	+	+++	+++	++
PARTITION-ABLE NV SRAM		+++	++	+	+++	+++	++
PSEUDO STATIC	+	+		++	+	+++	
FLASH	++	++	++	++	++	+	++
EEPROM	+	++	+	+		+	+
EPROM	++	++	++	++	+		++
OTP EPROM	+++	+++	+++	+++	+		+++
ROM	+++	+++	+++	+++	+		+++

+ = Degree of excellence

TYPES OF MEMORY

Many types of memories have been devised to meet varying application needs. However, nonvolatile read/write random access memories can be substituted for all memory types independent of application, if cost is not a primary consideration.

DRAM: Dynamic Random Access Memory. A DRAM, similar to an SRAM, stores information as a 1 or a 0. In an SRAM, this information is stored in a four to six transistor flip–flop which is easy to address, but requires a relatively large memory cell. A DRAM, by comparison, stores its 1 or 0 as a charge on a small capacitor, requir-

ing much more current then an SRAM to maintain the stored data. The net memory cell size is smaller for the DRAM than for the SRAM, so the total cost per bit of memory is less. The DRAM's capacitors must be constantly refreshed so that they retain their charge. DRAMs require more sophisticated interface circuitry.

SRAM: Static Random Access Memory. An SRAM is essentially a stable DC flip–flop requiring no clock timing or refreshing. The contents of an SRAM memory are retained as long as power is supplied. SRAMs support extremely fast access times. SRAMs also have relatively few strict timing requirements and a parallel address structure, making them particularly suited for cache and other low–density, frequent–access applications.

NV SRAM: Nonvolatile Static Random Access Memory. An NV SRAM is a single package which contains a low–power SRAM, a nonvolatile memory controller, and a lithium type battery. When the power supply to this single modular package falls below the minimum requirement to maintain the contents of the SRAM, the memory controller in the module switches the power supply from the external source to the internal lithium battery and write protects the SRAM. These transitions to and from the external power source are transparent to the SRAM, making it a true nonvolatile memory. This unique construction combines the strategic advantages of SRAM–addressing structure, high–speed access, and timing requirements–with the nonvolatility advantages of EEPROM technologies. Battery–backed SRAM modules from Dallas Semiconductor are pin–compatible with non–battery–backed SRAMs, making them ideal for any application where a traditional SRAM would be suitable.

PARTITIONABLE NV SRAM: A partitionable Dallas Semiconductor NV SRAM offers the same nonvolatility, addressing structure, and timing requirements of a regular Dallas Semiconductor NV SRAM product with the additional ability to write–protect selected blocks of memory, regardless of V_{CC}. This write protection feature requires no additional pins, and is instead controlled by a unique combination of read cycles (see DS1630, DS1645 and DS1650 data sheets). This feature allows a designer to configure a battery backed SRAM as both a RAM and a ROM–in one device. Because no additional pins are required for control, partitionable devices can be substituted for non–partitionables in existing designs, without making costly hardware changes.

PSEUDO STATIC RAM: Pseudo Static Random Access Memory. The advantages of using a Static RAM are the simplicity of the interface circuitry required, and the fact that the device is by nature "static," not requiring periodic refreshing to retain its data. A DRAM, however, provides lower cost–per–bit advantages and a higher memory density. A Pseudo–static RAM combines the advantages of the SRAM and DRAM by using dynamic storage cells to retain memory, and by placing all the required refresh logic on–chip so that the device functions similarly to an SRAM.

FLASH: A flash memory combines the electrical erase capability of an EEPROM with a cell that is similar to an EPROM. The result is that the modified cell may be block erased electrically instead of with UV light. This feature allows a Flash memory to accept new code updates or information while it is functioning in a system.

EEPROM: Electrically Erasable/Programmable Read Only Memory. A significant disadvantage of the EPROM memory is the fact that it cannot be reprogrammed while in a system. EPROM requires an external programming device to receive new code or data. An EEPROM eliminates this problem by providing a write function which can be used while the EEPROM is still in a circuit. A tradeoff for obtaining the write function while the EEPROM is still in a circuit is having to provide a high voltage (12.5V or above) source for the EEPROM when writing new data, or buying a more expensive EEPROM which has a charge pump in its package that allows it to be used with a standard 5 to 7V input. Although nonvolatile, EEPROM memory cells exhibit slow read/write access rates, making them most suitable for systems where performance is not an issue. The other read/write capable memories listed in Figure 1 provide the ability to frequently read and write data continuously over their entire lifetimes, in excess of 10 years, while EEPROM memory cells can rarely be rewritten more than 10,000 times. An EEPROM can be placed in a system and accessed as a standard RAM.

EPROM: Electrically Programmable Read Only Memory. An EPROM is a nonvolatile memory which offers the ability to both program and erase the contents of the memory multiple times. An EPROM must be programmed using a 12.5 volt (or higher) PROM programmer, and then transferred into the system in which it is intended to function. EPROMs can be erased by shining ultraviolet light into the window in the top of the IC package. The process of writing data into an EPROM and then erasing it may be repeated almost indefinitely.

EPROMs are usually used for product development, and later replaced with less expensive one–time programmable EPROMs.

OTP EPROM: One–Time Programmable EPROM. An EPROM which can only be written with code/data once instead of multiple times. Generally, OTP EPROMs are less expensive then erasable EPROMs.

ROM: Mask Programmable Read Only Memory. Mask programmable ROMs are the most durable form of memory storage. They are, however, "read only" and offer fairly slow performance. If a design has code/data that is very stable and will not need to be changed, a custom mask for the IC die can be made which will significantly reduce the cost of the ROM. A drawback to using a mask ROM is the significant cost penalty that must be incurred if an error in the code/data being stored forces a mask set change. The OTP EPROM fills the gap between ROM applications (no changes) and EPROMs (frequent changes).

MEETING APPLICATIONS NEEDS

NMOS DRAM memory provides performance and density, but, on the down side, must be constantly refreshed to retain data. At the opposite extreme are ROMs, offering nonvolatility and density, but lacking the ability to be updated with new data because information is programmed in only once. Between these two are a wide range of devices that fulfill some characteristics of the ideal memory.

Two popular devices, EEPROMs and Shadow RAMs, are designed to emulate a static RAM but also have the ability to retain data after a power loss. But despite their capability to retain data, both EEPROMs and Shadow RAMs fall short of meeting the industry's needs for several reasons.

Most notably, the EEPROM requires a special slow write cycle. The EEPROM's inability to support standard write cycle rates hinders performance in applications where memory is updated immediately as new data is available.

Another problem with EEPROMs is their wear–out mechanisms. These raise longevity concerns due to the limited number of write cycles allowed – sometimes as few as 10,000. If a static RAM with a 200 ns cycle time had this limitation, it would wear out in a mere 20 ms. In an application that requires constant updating, such as the buffer memory of a cashier's checkout terminal or a printer, the EEPROM's wear out mechanism is not acceptable.

Finally, because of the complexity of programming circuits, the cell structure and the special process technology required, the density of EEPROMs has not kept up with industry demands.

In systems requiring store–and–forward data, the memory must provide the desired fast write cycle as well as protection of data in the event of a power loss. Despite the promise of such a memory device and the effort invested by the industry, the ideal memory remains elusive.

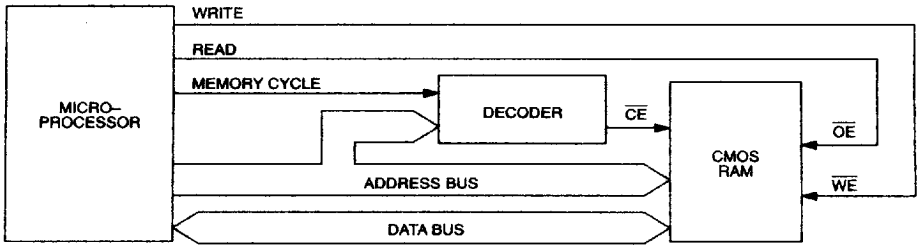
To more nearly emulate the ideal memory, Dallas Semiconductor combines its intelligent CMOS control circuitry (DS1210), a lithium energy source, and a very low power SRAM to offer a high density, nonvolatile memory.

Many Dallas devices, including the DS1220 (2K x 8 bits), DS1225 (8K x 8 bits), DS1230 (32K x 8 bits), DS1245 (128K x 8 bits), and DS1250 (512K x 8), use this fusion of technologies to provide a nonvolatile random access memory solution in densities up to 4096K bits.

CMOS NV SRAMs currently available have read and write cycle times of 70 ns, which exceeds most system requirements. They are much more robust than EEPROM, because there is no wear–out mechanism or write cycle limitation.

NV SRAMs are also the easiest to use and interface because the pinout configurations are standard throughout the industry. In fact, X8 or bytewide NV SRAMs can be interfaced directly to microprocessors (Figure 2). In addition, CMOS NV SRAMs offer low power in both active and standby modes, a characteristic sought by many designers. In most designs, memories remain in standby much of the time, keeping power consumption negligible. In the standby mode, current drain consists only of leakage currents in the tens of nanoamperes.

BYTEWIDE RAM TO MICROPROCESSOR INTERFACE Figure 2



BYTEWIDE MEMORIES PROVIDE EASY INTERFACE TO MICROPROCESSORS BECAUSE OF THE X8 ORGANIZATION AND CONTROL SIGNAL DEFINITION.

PUTTING LITHIUM AND RAM TOGETHER

The minute leakage currents of modern CMOS SRAMs can be sustained with a backup energy source to yield a most attractive nonvolatile memory. However, the actual solution involves more than just a CMOS memory and back up energy source (see Figure 3).

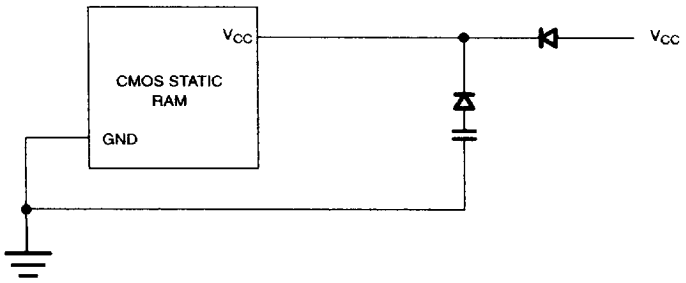
Battery backup design schemes are many and varied. The increase in density and availability of low–power CMOS memories in recent years has made this approach even more attractive. Yet problems still exist with battery backup design due to battery packaging and a lack of appropriate standard components to implement the support circuitry. One problem is providing isolation between the battery and power supply (see Figure 4). Diodes can provide isolation but produce a voltage drop which requires nonstandard power supplies and also subtracts from the battery voltage. A second problem is that the circuitry must be powered from the battery. Unless these devices draw an extremely modest amount of current, battery selection changes drastically. In fact, a current drain of even a couple of microamperes dictates the use of either rechargeable batteries or a replaceable battery scheme. If rechargeable batteries are selected, the recharging circuit can be costly and complex, and the best rechargeable battery cannot compare with the electrochemical stability of the lithium primary cell. Even worse, replaceable batteries add maintenance and cost to an in–service system. Battery packaging has also been a serious limitation, taking up valuable space and requiring special handling consideration to prevent discharge.

Dallas Semiconductor overcomes these obstacles by using high–capacity, non–rechargeable lithium batteries in its battery backed SRAMs.

ENERGY SOURCE

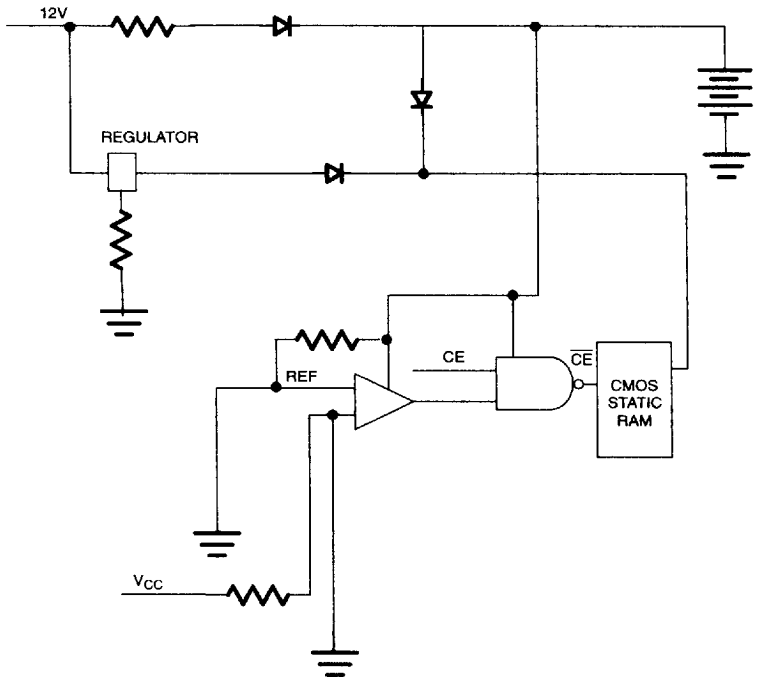
The energy source used to retain data in memory must be capable of outlasting the usefulness of the end product. Dallas Semiconductor NV SRAM products use an extremely stable electrochemical system with enough energy to guarantee a shelf life greater than 10 years.

BATTERY BACKUP CIRCUIT Figure 3



CMOS STATIC RAM REQUIRES MORE THAN JUST A BACKUP POWER SUPPLY. DATA MUST ALSO BE PROTECTED DURING POWER TRANSIENTS TO AVOID GARBLED DATA.

POWER SUPPLY AND BATTERY ISOLATION CIRCUITRY Figure 4



SUPPORT CIRCUITRY REQUIRED TO PRODUCE POWER FAIL DETECTION AND WRITE PROTECTION FORCES THE NEED FOR MULTICELL RECHARGEABLE BATTERY OR A LITHIUM BATTERY.

LITHIUM BATTERY BACKUP IS MORE RELIABLE

The lithium energy cell has raised concern about reliability and has been the object of much study. Data taken on the energy cell used in Dallas Semiconductor NV SRAMs indicates a cell failure rate less than 0.5% at 55°C over a 10 year period.

Additional life studies taken on the same lithium energy source encapsulated in Dallas Semiconductor's NV SRAMs have produced no failures in over 12 million device hours at 85°C. The lithium energy cell, then, is ideal for commercial and industrial semiconductor applications.

RETROFITTING EXISTING DESIGNS

The pinout of Dallas Semiconductor NV SRAMs is an established industry standard (Figure 9). The Joint Electronic Devices Engineering Council's Bytewide Version B Standard defines and upgrades from 2K x 8 in density to 128K x 8.

This standard accommodates RAM, ROM, UV EPROMs, and EEPROMs. Because of the flexibility and upgradeability of bytewide memories, the number of existing sockets is in the hundreds of millions. Therefore, many system designs can accommodate direct replacement of RAMs, EPROMs, ROMs, and EEPROMs with Dallas Semiconductor NV SRAMs. These solutions add real–time programmability and/or density upgrades to existing systems without redesign. Real–time programmability gives the system the ability to be personalized by the end user. In other words, NV SRAMs can be retrofitted into existing designs without making changes to existing hardware. This retrofitting offers a cost–effective, practical solution for companies who have invested in other memory devices that are less than ideal for their needs. For example, a design using conventional static RAM can be upgraded to nonvolatile memory by substituting a Dallas Semiconductor NV SRAM for the Static RAM memory.

IN–CIRCUIT PROGRAMMABILITY

The advantages of NV SRAM can be related to the capability of software. Modern systems seek customization for the cost of standard product. In this aspect, software can be adapted in a system to perform specialized functions. It is even possible to totally modify a system personality over the telephone. In–circuit programming also reduces maintenance cost by eliminating service calls to update software. Software stored in NV SRAM can be updated as often as necessary, depending on the configuration or application of the system.

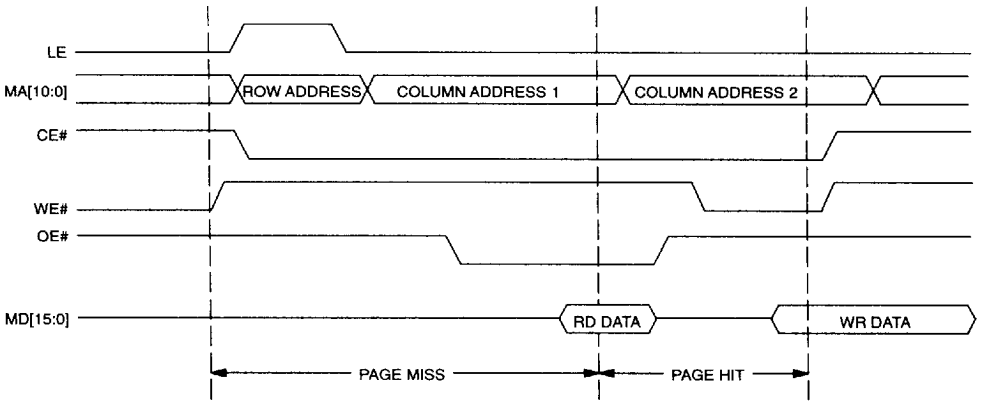
PORTABLE APPLICATIONS

The advancement of high density, low–power portable computers is continuing to drive development requirements. Difficult interface circuitry and refresh requirements of DRAM memories make them unsuitable for such applications. SRAMs are not only easier to address and consume less power when operating, but also require very little power to maintain the contents of their memory. Even better, an NV SRAM can provide the high performance of a DRAM or SRAM and also guarantee that the memory is truly nonvolatile. When a portable PC needs to be in standby mode, the memory can be powered down altogether.

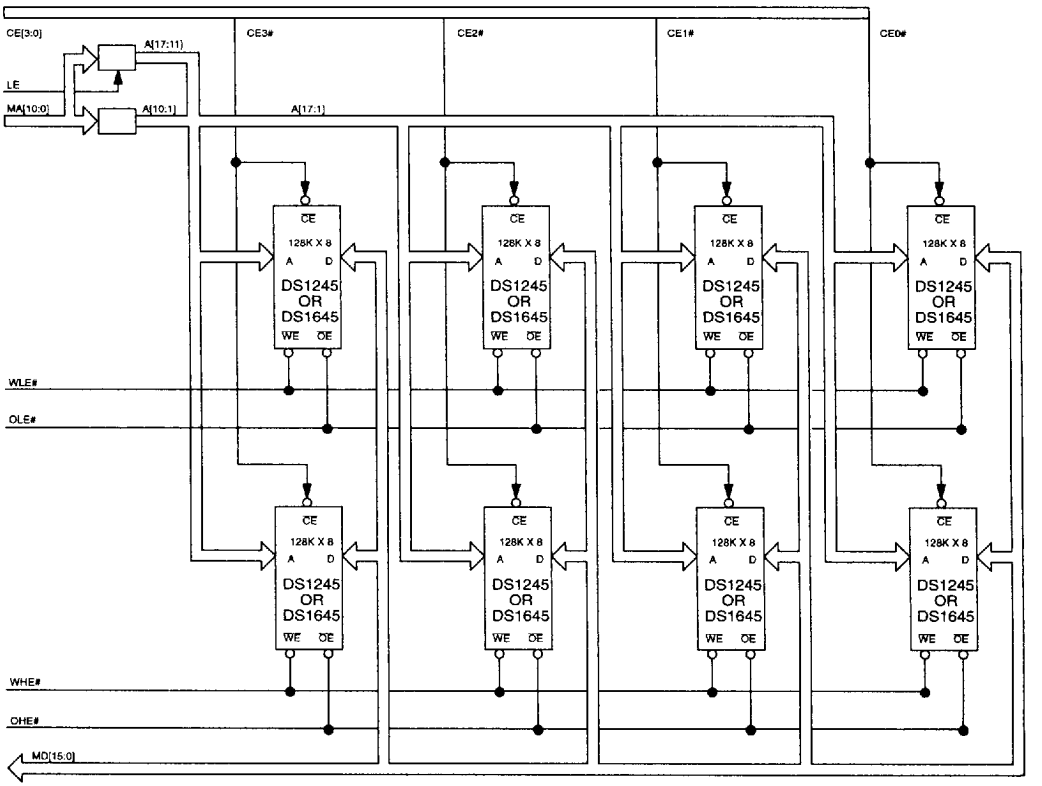
1 MBYTE MEMORY SUBSYSTEM USING NV SRAMs

Figure 6 shows a system block diagram with an Intel 386SL microprocessor with a 1 megabyte main memory of 128K x 8 NV SRAMs (DS1245). Figure 5, Portable Applications: Intel 386SL CPU/NV SRAM Timing, shows the requisite timing for the memory subsystem. The Intel 386SL is one of many microprocessors specially designed for low power, portable applications, and for addressing SRAM memory.

PORTABLE APPLICATIONS: INTEL 386SL CPU/NV SRAM TIMING Figure 5



1 MBYTE MEMORY SUBSYSTEM USING NV SRAMS Figure 6



In Figure 6, eight DS1245 SRAMs are used to create a four–bank 1Mbyte SRAM memory subsystem. The following signals from the Intel 386SL CPU are required to address the SRAM module based system. (The 386SL memory controller must be configured in its SRAM addressing mode for this application.)

LE: Latch Enable. This signal is active high and serves to indicate that a row address is to be put on the address bus. A row address must be latched at this signal's falling edge. LE is connected to the latch enable input of the address latch.

MA[10:0]: Multiplexed Memory Address Bus. This bus provides address information for the Memory Controller Unit. The bus provides a 22 bit address in a multiplexed row/column sequence.

$\overline{CE}$[3:0]: Chip Enable outputs. These signals provide chip enable control for each SRAM bank.

$\overline{WLE}$: Write Low Enable. Indicates a write access to the lower byte of the 386SL CPU memory bus. The lower byte of data is put on the memory bus at the falling edge of $\overline{WLE}$.

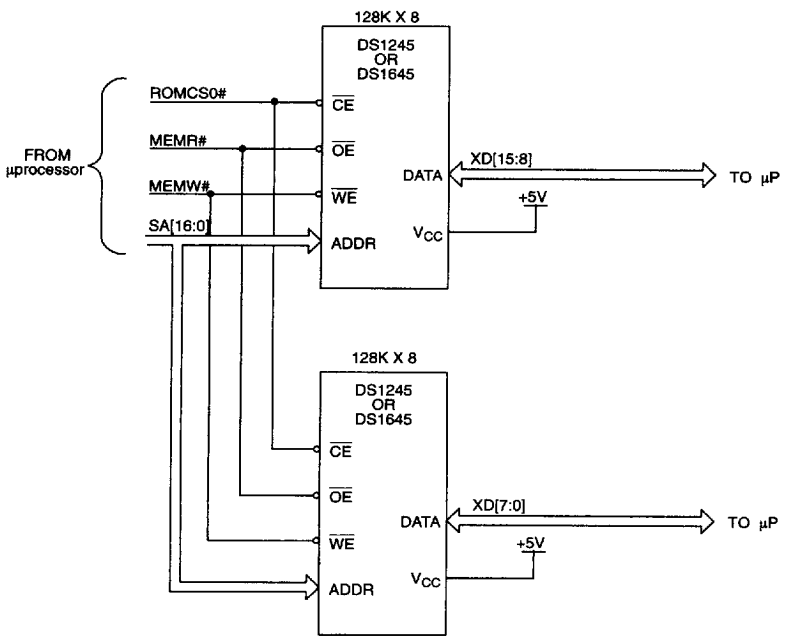
$\overline{WHE}$: Write High Enable. Indicates a write access to the high byte of the 386SL CPU memory bus. The high byte of data is put on the memory bus at the falling edge of $\overline{WHE}$.

$\overline{OLE}$: Output Low Enable. Enables the lower byte output from the NV SRAM modules.

$\overline{OHE}$: Output High Enable. Enables the high byte output from the NV SRAM modules.

MD[15:0]: Memory Data Bus. This bus provides data information for the Memory Controller Unit. Accesses from the Memory Controller Unit to the NV SRAM memory modules take place through this bus.

16–BIT SINGLE–BANK NV SRAM BIOS CIRCUIT Figure 7



16–BIT SINGLE–BANK NV SRAM BIOS CIRCUIT

Figure 7 shows Dallas NV SRAMs providing BIOS memory storage for an Intel 386SL CPU. Using the DS1645 NV SRAMs provides several advantages over using either OTP EPROM or FLASH memories.

Flash memories require more operating current than NV SRAMs. Flash memories also require a high voltage source, 12V+, for any writes or updates that must be made to BIOS. NV SRAMs, on the other hand, require only their standard V_{CC} 5V input for both read and write access. Like Flash memories, a DS1645 NV SRAM maintains the contents of its memory in the absence of V_{CC}. A DS1645 has the additional feature that it can be easily programmed to write protect user–selected blocks of memory. In effect, individual memory blocks in the NV SRAM module can be configured to appear as ROM memory, without detracting from the DS1645's ability to receive BIOS updates in its non–write–protected blocks of memory.

Traditional OTP EPROMs, while nonvolatile and very low–power like the DS1245 and DS1645 NV SRAMs, are lacking in that they can only be programmed once, and usually require a special fixture to be programmed. DS1245 and DS1645 NV SRAMs provide the capability to update BIOS repeatedly without removing them from the system. DS1245 and DS1645 NV SRAMs also provide fast 70 ns access times, negating the need to insert additional wait states into BIOS access timing requirements.

The signals shown in Figure 7 are taken directly from the Intel 386SL CPU:

ROMCSO#: This signal is a dedicated ROM control signal provided by the 386SL CPU. It is active low and is used to enable the system BIOS.

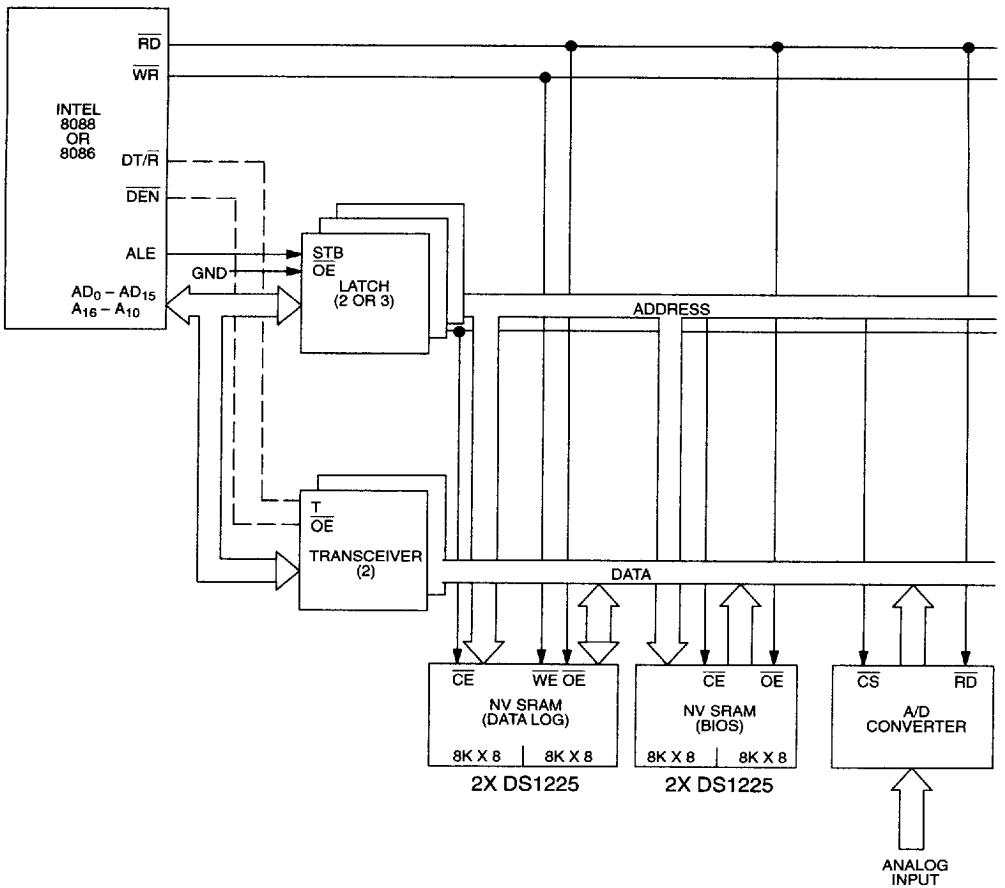
MEMR#: Memory Read. This signal indicates when a memory read access is occurring on the ISA bus and is active low.

MEMW#: Memory Write. This signal indicates when a memory write access is occurring on the ISA bus and is active low.

XD[15:0]: X–bus Data. Buffered data lines from the system data bus. These signals are produced using an external transceiver (see Intel 386SL Superset System Design Guide).

SA[16:0]: System Address Bus. This bus is driven by the 386SL CPU for system I/O accesses.

DATA LOGGING Figure 8



DATA LOGGING

Figure 8 shows how Dallas Semiconductor's NV SRAMs can provide a special advantage in environments where the power supply is not entirely reliable, or when power must periodically be shut down. Dallas Semiconductor NV SRAMs contain memory control circuitry which not only maintains the data in the SRAM in the absence of power, but also write protects the device if V_{CC} is out of tolerance. This feature ensures that an unstable power supply does not corrupt data which has been collected.

In this application, an Intel 8086 is shown in its minimal mode, connected to an address latch and bus transceiver to demultiplex the 8086's bus (see Figure 8). The resulting address and data busses may then be connected directly to two memory banks, one 8K x 16 BIOS memory consisting of two DS1225 NV SRAMs, the other an 8K x 16 memory bank consisting of two DS1225's acting as a data log. A data collecting device, such as an A/D converter, can be addressed as a read–only peripheral device to sample a value and write it to the DS1225 acting as a data log. The DS1225s acting as the data log can transmit their data on the data bus to another peripheral, or may be removed from the system and taken to another location to have the log extracted.

DALLAS SEMICONDUCTOR BATTERY BACKUP SRAM MODULES Figure 9