1103

1024×1 DYNAMIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION – The 1103 is a fully decoded 1024-word by 1-bit Dynamic Random Access Memory, especially suited for main memory applications. The circuitry is designed for maximum speed and low standby power dissipation. It requires two power supplies and two clocks including the Chip Enable ($\overline{CE}$). Readout is non destructive and the Data Out can be wired-OR for ease of expansion. Exercise of the 32 row addresses is required for refresh.

The 1103 is manufactured with the p-channel Isoplanar process. It is available in 18-pin ceramic Dual In-line Packages in the commercial temperature range.

- **FAST ACCESS (120, 150, 220 AND 300 ns)**
- **LOW POWER**
- **FULLY EXPANDABLE**
- **FULLY DECODED**
- **WIRED-OR CAPABILITY**
- **18-PIN CERAMIC DUAL IN-LINE PACKAGE**

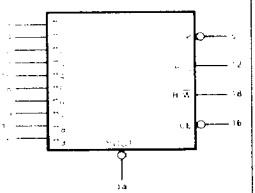
PIN NAMES

A_n	Address Inputs
D_{IN}	Data Input
$\overline{D_{OUT}}$	Data Output
$\overline{CE}$	Chip Enable
$R/\overline{W}$	Read/Write
P	Precharge

ABSOLUTE MAXIMUM RATINGS

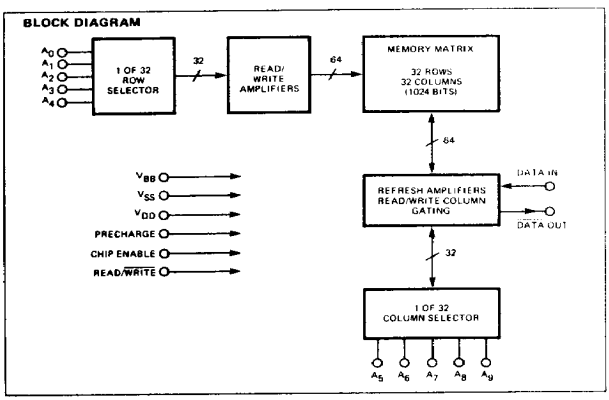
All Pins with Respect to V_{BB} −25 V to +0.3 V
Storage Temperature −55°C to +150°C
Operating Temperature: 1103-1, 1103S, 1103F 0°C to +55°C
1103 0°C to +70°C

LOGIC SYMBOL

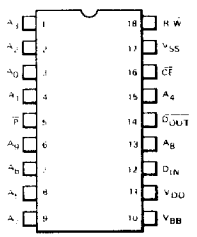


V_{BB} = Pin 10
V_{SS} = Pin 17
V_{DD} = Pin 11

BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



DC REQUIREMENTS: 1103F, T_A = 0°C to +55°C; **1103**, T_A = 0°C to +70°C

SYMBOL	PARAMETER	1103F MIN	1103F MAX	1103 MIN	1103 MAX	UNITS	CONDITIONS
V_{SS}	Positive Supply Voltage	18	20	15.2	16.8	V	
V_{BB}	Bias Supply Voltage	V_{SS}+3	V_{SS}+4	V_{SS}+3	V_{SS}+4	V	
V_{DD}	Negative Supply Voltage	0	0	0	0	V	
V_{IH1}	Input HIGH Voltage	V_{SS}−1	V_{SS}+1	V_{SS}−1	V_{SS}+1	V	T_A = Min
V_{IH2}	Input HIGH Voltage	V_{SS}−1	V_{SS}+1	V_{SS}−0.7	V_{SS}+1	V	T_A = Max
V_{IL1}*	Input LOW Voltage (A)	V_{SS}−20	V_{SS}−18	V_{SS}−17	V_{SS}−14.2	V	T_A = Min
V_{IL2}*	Input LOW Voltage (A)	V_{SS}−20	V_{SS}−18	V_{SS}−17	V_{SS}−14.5	V	T_A = Max
V_{IL3}*	Input LOW Voltage (B)	V_{SS}−20	V_{SS}−18	V_{SS}−17	V_{SS}−14.7	V	T_A = Min
V_{IL4}*	Input LOW Voltage (B)	V_{SS}−20	V_{SS}−18	V_{SS}−17	V_{SS}−15	V	T_A = Max

*See waveforms input type

DC CHARACTERISITCS: 1103F, T_A = 0°C to +55°C; **1103**, T_A = 0°C to +70°C

SYMBOL	PARAMETER	1103F MIN	1103F MAX	1103 MIN	1103 MAX	UNITS	CONDITIONS
V_{OH1}	Output HIGH Voltage	115	700	60	400	mV	T_A = 25°C, Note 1
V_{OH2}	Output HIGH Voltage	90	700	50	400	mV	T_A = Max Operating Temperature, Note 1
V_{OL}	Output LOW Voltage						Note 2
I_{OH1}	Output HIGH Current	1150	7000	600	4000	µA	T_A = 25°C
I_{OH2}	Output HIGH Current	900	7000	500	4000	µA	T_A = Max Operating Temperature
I_{OL}	Output LOW Current						Note 2
I_{IN}	Input Load Current		10		1.0	µA	
I_{OUT}	Output Leakage Current		10		1.0	µA	
I_{BB}	V_{BB} Supply Current		100		100	µA	
I_{DD1}	Supply Current During t_{PC}		60		56	mA	
I_{DD2}	Supply Current During t_{OV}		68.5		59	mA	T_A = 25°C
I_{DD3}	Supply Current During t_{POV}		11		11	mA	
I_{DD4}	Supply Current During t_{CP}		4.0		4.0	mA	
I_{DDAV}	Average Supply Current		26		25	mA	T_A = 25°C, Note 3

1. Assumes a load resistor of 100 Ω.
2. The output current and voltage for LOW is a function of load resistor.
3. t_{RWC} = min. Precharge width at 50%: 1103F, 60 ns; 1103, 190 ns.

AC REQUIREMENTS: 1103F, T_A = 0°C to +55°C; **1103**, T_A = 0°C to +70°C

SYMBOL	PARAMETER	1103F MIN	1103F MAX	1103 MIN	1103 MAX	UNITS	CONDITIONS
t_{REF}	Time Between Refresh		2.0		2.0	ms	
t_{AC}	Address to Chip Enable Set-up Time	30		115		ns	
t_{CA}	Chip Enable to Address Hold Time	10		20		ns	
t_{PC}	Precharge to Chip Enable Delay	35		125		ns	
t_{CP}	Chip Enable to Precharge Delay	40		85		ns	
t_{OVL}	Precharge and Chip Enable Overlap LOW			25	75	ns	
t_{OVH}	Precharge and Chip Enable Overlap HIGH				140	ns	
t_{OVM}	Precharge and Chip Enable Overlap, 50% Points	13	50	45	95	ns	
t_{RC}	Read Cycle	238		480		ns	Note 4
t_{POV}	Precharge to End Chip Enable (Read Cycle)	114	700	165	500	ns	
t_{WC}	Write Cycle	270		580		ns	Note 4
t_{RWC}	Read/Write Cycle	270		580		ns	Note 4
t_{PW}	Precharge to Read/Write Delay	114	700	165	500	ns	
t_{WP}	Read/Write Pulse Width	20		50		ns	
t_W	Read/Write Set-up Time	20		80		ns	
t_{DW}	Data Set-up Time	25		105		ns	
t_{DH}	Data Hold Time	10		10		ns	
t_{CW}	Relationship between Chip Enable and Read/Write		5.0		0	ns	

4. Assumes t_T = 12 ns for 1103F, 20 ns for 1103.

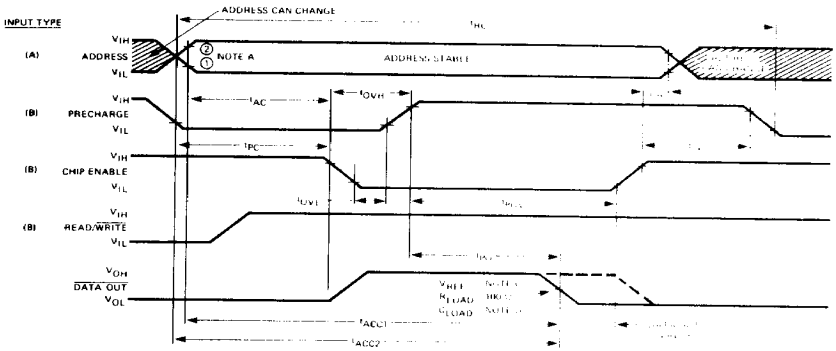
AC CHARACTERISTICS: **1103F**, T_A = 0°C to 55°C; **1103**, T_A = 0°C to +70°C

SYMBOL	PARAMETER	1103F MIN	1103F MAX	1103 MIN	1103 MAX	UNITS	CONDITIONS
t_{PO}	End of Precharge to Output Delay (See Waveforms)		65		120	ns	
t_{ACC1}	Address to Output Access		120		400	ns	Note 5
t_{ACC2}	Precharge to Output Access		125		310	ns	Note 6

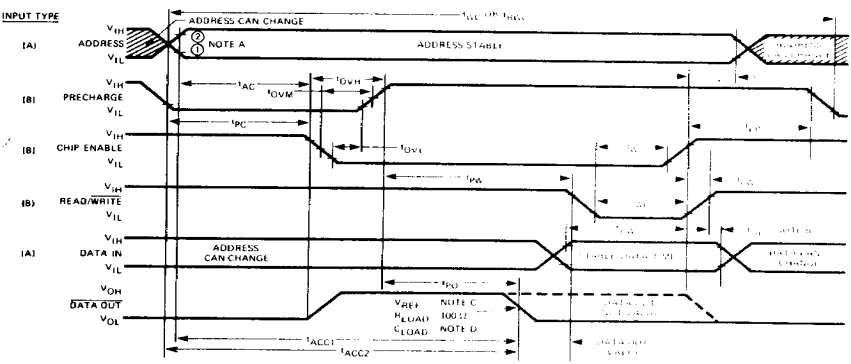
5. $t_{ACC1(max)} = t_{AC\ min} + t_{OVL\ min} + t_{PO\ max} + 2T_t$
6. $t_{ACC2\ (max)} = t_{PC\ min} + t_{OVL\ min} + t_{PO\ max} + 2T_t$

WAVEFORMS

READ CYCLE



WRITE CYCLE OR READ/WRITE CYCLE



NOTES:

A. Point ① = V_{DD} +2.0 V; Point ② = V_{SS} − 2.0 V } T_t is defined as the transitions between these two points

B. t_{DH} is referenced to point ② of the rising edge of Chip Enable or Read/Write, whichever occurs first.

C. V_{REF} = 80 mV (1103F,1103-1) , 40 mV (1103,1103S)

D. C_{LOAD} = 50 pF (1103F, 1103-1), 100 pF (1103, 1103S)

DC REQUIREMENTS: 1103-1 and 1103S, T_A = 0°C to +55°C

SYMBOL	PARAMETER	1103-1 MIN	1103-1 MAX	1103S MIN	1103S MAX	UNITS	CONDITIONS
V_{SS}	Positive Supply Voltage	18.05	19.95	18.05	19.95	V	
V_{BB}	Bias Supply Voltage	V_{SS}+3	V_{SS}+4	V_{SS}+3	V_{SS}+4	V	
V_{DD}	Negative Supply Voltage	0	0	0	0	V	
V_{IH1}	Input HIGH Voltage	V_{SS}−1	V_{SS}+1	V_{SS}−1	V_{SS}+1	V	T_A = 0°C
V_{IH2}	Input HIGH Voltage	V_{SS}−1	V_{SS}+1	V_{SS}−0.7	V_{SS}+1	V	T_A = 55°C
V_{IL1}*	Input LOW Voltage (A)	V_{SS}−20	V_{SS}−18	V_{SS}−20	V_{SS}−17	V	T_A = 0°C
V_{IL2}*	Input LOW Voltage (A)	V_{SS}−20	V_{SS}−18	V_{SS}−20	V_{SS}−17.3	V	T_A = 55°C
V_{IL3}*	Input LOW Voltage (B)	V_{SS}−20	V_{SS}−18	V_{SS}−20	V_{SS}−17	V	T_A = 0°C
V_{IL4}*	Input LOW Voltage (B)	V_{SS}−20	V_{SS}−18	V_{SS}−20	V_{SS}−17.3	V	T_A = 55°C

*See waveforms input type.

DC CHARACTERISITCS: 1103-1 and 1103S, T_A = 0°C to +55°C

SYMBOL	PARAMETER	1103-1 MIN	1103-1 MAX	1103S MIN	1103S MAX	UNITS	CONDITIONS
V_{OH1}	Output HIGH Voltage	115	700	60	700	mV	T_A = +25°C, Note 1
V_{OH2}	Output HIGH Voltage	90	700	50	700	mV	T_A = 55°C, Note 1
V_{OL}	Output LOW Voltage						Note 2
I_{OH1}	Output HIGH Current	1150	7000	600	7000	µA	T_A = 25°C
I_{OH2}	Output HIGH Current	900	7000	500	7000	µA	T_A = 55°C
I_{OL}	Output LOW Current						Note 2
I_{LI}	Input Load Current		10		10	µA	
I_{LO}	Output Leakage Current		10		10	µA	
I_{BB}	V_{BB} Supply Current		100		100	µA	
I_{DD1}	Supply Current During t_{PC}		60		60	mA	
I_{DD2}	Supply Current During t_{OV}		68.5		68.5	mA	T_A = 25°C
I_{DD3}	Supply Current During t_{POV}		11		11	mA	
I_{DD4}	Supply Current During t_{CP}		4.0		4.0	mA	
I_{DDAV}	Average Supply Current		26		24	mA	T_A = 25°C, Note 7

7. t_{RWC} = min; Precharge width at 50%: 1103-1, 105 ns, 1103S, 95 ns.

AC REQUIREMENTS: 1103-1 and 1103S, T_A = 0°C to +55°C

SYMBOL	PARAMETER	1103-1 MIN	1103-1 MAX	1103S MIN	1103S MAX	UNITS	CONDITIONS
t_{REF}	Time Between Refresh		1.0		1.0	ms	
t_{AC}	Address to Chip Enable Set-up Time	30		70		ns	
t_{CA}	Chip Enable to Address Hold Time	10		20		ns	
t_{PC}	Precharge to Chip Enable Delay	60		70		ns	
t_{CP}	Chip Enable to Precharge Delay	40		50		ns	
t_{OVL}	Precharge and Chip Enable Overlap LOW	5.0	30	5.0	45	ns	
t_{OVH}	Precharge and Chip Enable Overlap HIGH		85		105	ns	
t_{OVM}	Precharge and Chip Enable Overlap, 50% Points	25	50			ns	
t_{RC}	Read Cycle	300		345		ns	τ_t = 20 ns
t_{POV}	Precharge to End Chip Enable (Read Cycle)	115	500	140	500	ns	
t_{WC}	Write Cycle	340		390		ns	τ_t = 20 ns
t_{RWC}	Read/Write Cycle	340		390		ns	τ_t = 20 ns
t_{PW}	Precharge to Read/Write Delay	115	500	140	500	ns	
t_{WP}	Read/Write Pulse Width	20		25		ns	
t_W	Read/Write Set-up Time	20		25		ns	
t_{DW}	Data Set-up Time	40		45		ns	
t_{DH}	Data Hold Time	10		10		ns	
t_{CW}	Relationship between Chip Enable and Read/Write		0			ns	

AC CHARACTERISTICS: 1103-1 and 1103S, T_A = 0°C to +55°C

SYMBOL	PARAMETER	1103-1		1103S		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
t_{PO}	End of Precharge to Output Delay (See Waveforms)		75		105	ns	
t_{ACC1}	Address to Output Access		150		220	ns	Note 5
t_{ACC2}	Precharge to Output Access		180		220	ns	Note 6

CAPACITANCE CHARACTERISTICS (pF): All unused pins at AC ground, f_0 = 1 MHz, V_{BB} = +3.0 Volts

SYMBOL	CAPACITANCE	1103, 1103-1, 1103S, 1103F		CONDITIONS
		TYP	MAX	
C_{AD}	Address	6.0	8.0	V_{IN} = V_{SS}
C_{PR}	Precharge	19	23	V_{IN} = V_{SS}
C_{CE}	Chip Enable	15	18	V_{IN} = V_{SS}
C_{RW}	Read/Write	15	18	V_{IN} = V_{SS}
C_{IN}	Data Input	5.0	7.0	Chip Enable = V_{DD} or V_{SS}, V_{IN} = V_{SS}
C_{OUT}	Data Output	3.0	4.0	V_{OUT} = V_{DD}

3