

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40097B

buffers

3-state hex non-inverting buffer

Product specification
File under Integrated Circuits, IC04

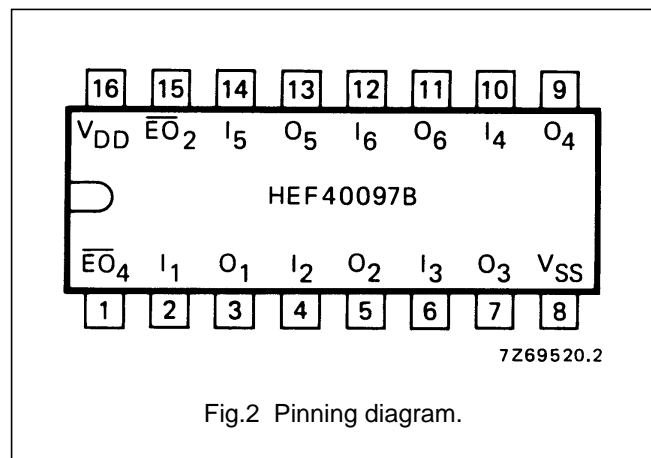
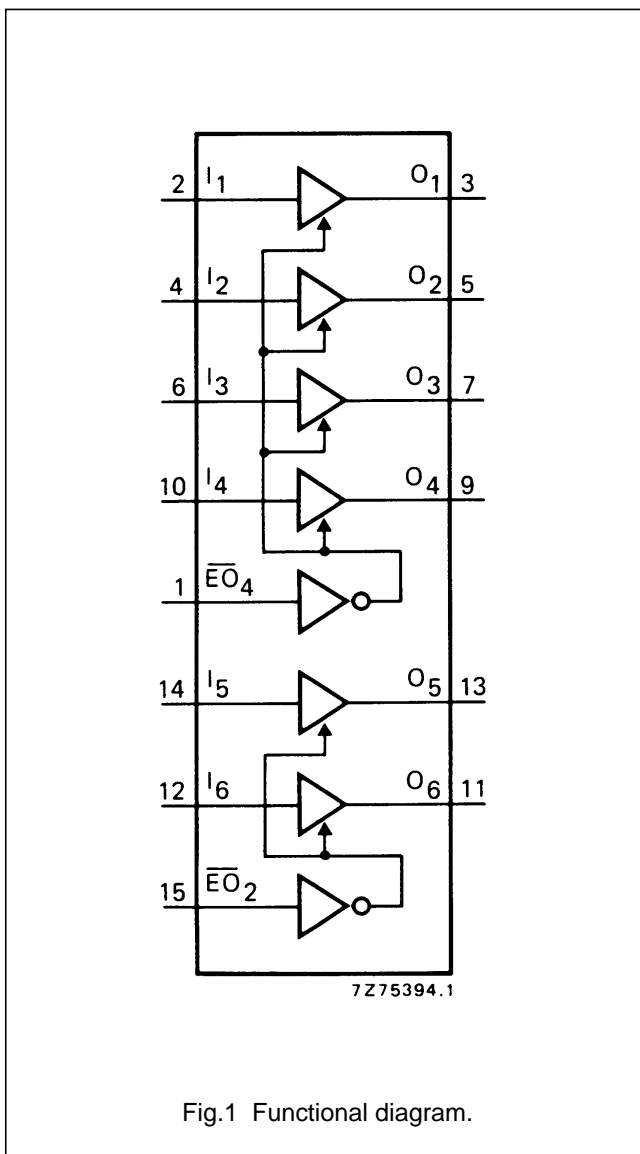
January 1995

3-state hex non-inverting buffer

HEF40097B buffers

DESCRIPTION

The HEF40097B is a hex non-inverting buffer with 3-state outputs. The 3-state outputs are controlled by two enable inputs (\overline{EO}_4 and \overline{EO}_2). A HIGH on \overline{EO}_4 causes four of the six buffer elements to assume a high impedance or OFF-state, regardless of the other input conditions and a HIGH on \overline{EO}_2 causes the outputs of the remaining two buffer elements to assume a high impedance or OFF-state, regardless of the other input conditions.



- HEF40097BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF40097BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF40097BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

PINNING

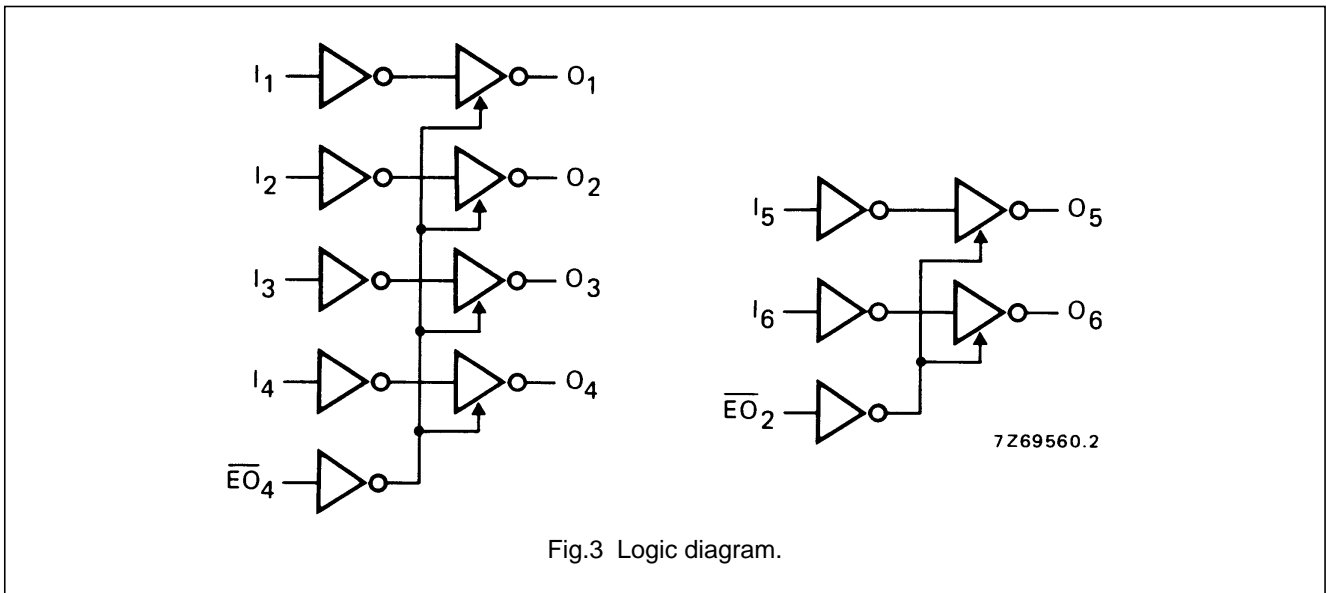
- I_1 to I_6 buffer inputs
- \overline{EO}_4 , \overline{EO}_2 enable inputs (active LOW)
- O_1 to O_6 buffer outputs (active HIGH)

FAMILY DATA, I_{DD} LIMITS category BUFFERS

See Family Specifications

3-state hex non-inverting buffer

HEF40097B
buffers



DC CHARACTERISTICS

V_{SS} = 0 V

HEF	V _{DD} V	V _{OH} V	V _{OL} V	SYMBOL	T _{amb} (°C)					
					-40		+25		+85	
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Output current HIGH	5	4,6		-I _{OH}	1,2	1,0	0,8	mA		
	10	9,5			3,8	3,2	2,5	mA		
	15	13,5			12,0	10,0	8,0	mA		
HIGH	5	2,5		-I _{OH}	3,8	3,2	2,5	mA		
Output current LOW	4,75		0,4	I _{OL}	3,5	2,9	2,3	mA		
	10		0,5		12,0	10,0	8,0	mA		
	15		1,5		24,0	20,0	16,0	mA		

HEC	V _{DD} V	V _{OH} V	V _{OL} V	SYMBOL	T _{amb} (°C)					
					-55		+25		+125	
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Output current HIGH	5	4,6		-I _{OH}	1,25	1,0	0,6	mA		
	10	9,5			4,0	3,2	2,1	mA		
	15	13,5			12,5	10,0	6,7	mA		
HIGH	5	2,5		-I _{OH}	4,0	3,2	2,1	mA		
Output current LOW	4,75		0,4	I _{OL}	3,6	2,9	1,9	mA		
	10		0,5		12,5	10,0	6,7	mA		
	15		1,5		25,0	20,0	13,0	mA		

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AC CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	70	140	ns	60 ns + (0,20 ns/pF) C_L
	10		30	60	ns	26 ns + (0,08 ns/pF) C_L
	15		25	50	ns	22 ns + (0,06 ns/pF) C_L
LOW to HIGH	5	t_{PLH}	60	120	ns	45 ns + (0,30 ns/pF) C_L
	10		25	50	ns	19 ns + (0,13 ns/pF) C_L
	15		20	40	ns	16 ns + (0,09 ns/pF) C_L
Output transition times HIGH to LOW	5	t_{THL}	30	60	ns	15 ns + (0,30 ns/pF) C_L
	10		15	30	ns	10 ns + (0,11 ns/pF) C_L
	15		10	20	ns	7 ns + (0,07 ns/pF) C_L
LOW to HIGH	5	t_{TLH}	35	70	ns	10 ns + (0,50 ns/pF) C_L
	10		20	40	ns	8 ns + (0,24 ns/pF) C_L
	15		15	30	ns	6 ns + (0,18 ns/pF) C_L
3-state propagation delays Output disable times $\overline{EO}_2, \overline{EO}_4 \rightarrow O_n$ HIGH	5	t_{PHZ}	45	95	ns	
	10		35	70	ns	
	15		30	60	ns	
LOW	5	t_{PLZ}	60	120	ns	
	10		35	70	ns	
	15		25	55	ns	
Output enable times $\overline{EO}_2, \overline{EO}_4 \rightarrow O_n$ HIGH	5	t_{PZH}	75	150	ns	
	10		35	70	ns	
	15		30	60	ns	
LOW	5	t_{PZL}	95	190	ns	
	10		40	80	ns	
	15		30	65	ns	

	V_{DD} V	TYPICAL FORMULA FOR P (μ W)	
Dynamic power dissipation per package (P)	5	$5\ 400 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$25\ 200 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$96\ 500 f_i + \sum (f_o C_L) \times V_{DD}^2$	