National Semiconductor

2900 Family/
Bipolar Microprocessor

IDM2901A, IDM2901A-1/IDM2901A-2
4-Bit Bipolar Microprocessor

General Description

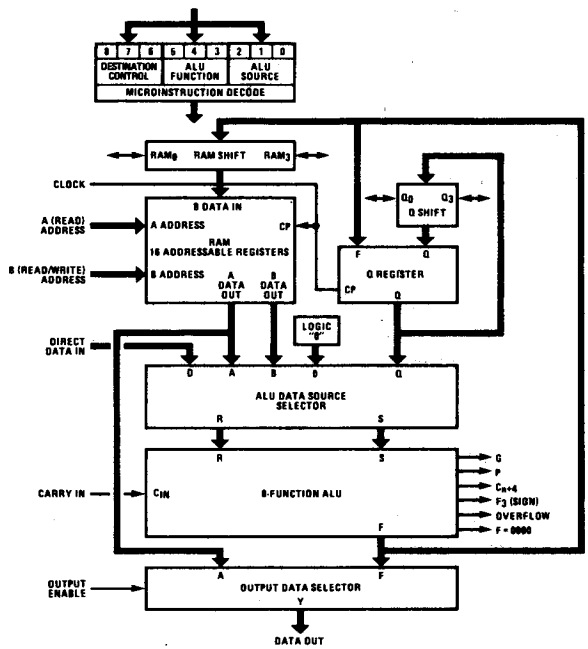
The IDM2901 4-bit bipolar microprocessor slice is a cascadable device designed for use in Central Processing Units, programmable microprocessors, peripheral controllers, and other "high-speed" applications where economy, hardware/software flexibility, and easy expansion are system prerequisities. The building-block architecture and microinstruction format of the IDM2901 permit efficient emulation of most digital-based systems.

As shown in the simplified block diagram, the IDM2901 device consists of a 16-word by 4-bit 2-port RAM, a high-speed ALU, and the required shifting, decoding, and multiplexing circuits. The 9-bit microinstruction word is organized into three groups of three bits each – the first group (bits 0 - 2) selects ALU source operands, the second group (bits 3 - 5) selects the ALU function, and the last group (bits 6 - 8) selects the destination register within the ALU. The slice microprocessor is cascadable with full look-ahead or ripple carry; all outputs are TRI-STATE® and four status-flag outputs are available. To minimize power consumption and to maximize speed and reliability, the 40-pin LSI chip is fabricated using a National state-of-the-art Low-Power Schottky technology called "SCL".

Features and Benefits

- **Multiple-address architecture** – improves system speed by providing simultaneous yet independent access to two working registers.
- **Multifunction ALU** – performs addition, two subtraction operations, and five logic functions on two source operands.
- **Flexible data-source selection** – for every ALU function, data is selected from five source ports for a total of 203 source operand pairs.
- **Left/right shift independent of ALU** – an arithmetic operation and a left or right shift can be obtained on the same machine cycle.
- **Four status flags** – carry, overflow, zero, and functional sign are available as outputs.
- **Expandable** – Connect any number of IDM2901s together for longer word lengths.
- **Microprogrammable** – three groups of 3 bits each for source operand, ALU function, and destination control.

Block Diagram



Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +6.3 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

Operating Range

P/N	Temperature	V_{CC}
IDM2901 JC, NC	T_A = 0°C to +70°C	4.75V to 5.25V
IDM2901 JM, JM/883	T_C = −55°C to +125°C	4.50V to 5.50V
IDM2901A-1 JC, NC	T_A = 0°C to +70°C	4.75V to 5.25V
IDM2901A-1 JM, JM/883	T_C = −55°C to +125°C	4.50V to 5.50V

Standard Screening (Conforms to MIL-STD-883 for Class C parts)

Step	MIL-STD-883 Method	Conditions	Level JC, NC	Level JM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C: 24-hour 150°C	100%	100%
Temperature Cycle	1010	C: −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B: 10,000 G	100%*	100%
Fine Leak	1014	A: 5 x 10^{-8} atm-cc/cm^3	100%*	100%
Gross Leak	1014	C2: Fluorocarbon	100%*	100%
Electrical Test Subgroups 1 and 7 and 9	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B Parts				
Group A Sample Tests				
Subgroup 1	5005	See below for definitions of subgroups	LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 5
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 5

*Not applicable to IDM2901ANC.

Additional Screening for Class B Parts

Step	MIL-STD-883 Method	Conditions	Level JM/883
Burn-In	1015	D: 125°C, 160 hours min	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

Group A Subgroups

(as defined in MIL-STD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum rated temperature
11	Switching	Minimum rated temperature

Electrical Characteristics Over Operating Range IDM2901A/IDM2901A-1

Symbol	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output High Voltage	V_{CC} = min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6 mA; $Y_0/Y_1/Y_2/Y_3$	2.4			V
			I_{OH} = −1.0 mA; C_{n+4}	2.4			
			I_{OH} = −800 μA; OVR/P	2.4			
			I_{OH} = −600 μA; F_3	2.4			
			I_{OH} = −600 μA; $RAM_{0,3}/Q_{0,3}$	2.4			
			I_{OH} = −1.6 mA; $\overline{G}$	2.4			

Electrical Characteristics (cont'd.)

Symbol	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
I_{CEX}	Output Leakage Current for F = 0 Output	V_{CC} = min; V_{OH} = 5.5 V, V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output Low Voltage	V_{CC} = min; V_{IN} = V_{IH} or V_{IL}		I_{OL} = 20 mA (Com'l) $Y_0/Y_1/Y_2/Y_3$			0.5	V
				I_{OL} = 16 mA (Mil); $Y_0/Y_1/Y_2/Y_3$			0.5	
				I_{OL} = 16 mA; $\overline{G}/F$ = 0			0.5	
				I_{OL} = 10 mA; C_{n+4}			0.5	
				I_{OL} = 10 mA; OVR/$\overline{P}$			0.5	
				I_{OL} = 8 mA; $F_3/RAM_{0,3}/Q_{0,3}$			0.5	
V_{IH}	Input High Level	Guaranteed input logical high voltage for all inputs			2.0			V
V_{IL}	Input Low Level	Guaranteed input logical low voltage for all inputs					0.8	V
V_I	Input Clamp Voltage	V_{CC} = min; I_{IN} = −18 mA					−1.5	V
I_{IL}	Input Low Current	V_{CC} = max; V_{IN} = 0.5 V		Clock/$\overline{OE}/C_n$			−0.36	mA
				$A_0/A_1/A_2/A_3$			−0.36	
				$B_0/B_1/B_2/B_3$			−0.36	
				$D_0/D_1/D_2/D_3$			−0.36	
				$I_0/I_1/I_2/I_6$			−0.36	
				$I_3/I_4/I_5$			−0.36	
				I_7/I_8			−0.36	
				$RAM_{0,3}/Q_{0,3}$ (Note 4)			−0.36	
I_{IH}	Input High Current	V_{CC} = max; V_{IN} = 2.7 V		Clock/OE			20	μA
				$A_0/A_1/A_2/A_3$			20	
				$B_0/B_1/B_2/B_3$			20	
				$D_0/D_1/D_2/D_3$			20	
				$I_0/I_1/I_2/I_6/I_8$			20	
				$I_3/I_4/I_5/I_7$			20	
				$RAM_{0,3}/Q_{0,3}$ (Note 4)			100	
				C_n			20	
I_I	Input High Current	V_{CC} = max; V_{IN} = 5.5 V					1.0	mA
I_{OZH}, I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = max	$Y_0/Y_1/Y_2/Y_3$	V_O = 2.4 V			50	μA
				V_O = 0.5 V			−50	
			$RAM_{0,3}/Q_{0,3}$	V_O = 2.4 V (Note 4)			100	
				V_O = 0.5 V (Note 4)			−360	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = 5.75 V, V_O = 0.5 V	$Y_0/Y_1/Y_2/Y_3/\overline{G}$		−30		−85	mA
			C_{n+4}		−30		−85	
			OVR/$\overline{P}$		−30		−85	
			F_3		−30		−85	
			$RAM_{0,3}/Q_{0,3}$		−30		−85	
I_{CC}	Power Supply Current (Note 6)	V_{CC} = max		T_A = 25°C		160	245	mA
			JC	T_A = 0°C to +70°C		160	260	mA
				T_A = +70°C		160	220	
			JM	T_C = −55°C to +125°C		160	275	
				T_C = +125°C		160	185	

Note 1: For conditions shown as min or max, use the appropriate value specified under Electrical Characteristics for the applicable device type.

Note 2: Typical limits are at V_{CC} = 5.0 V, 25°C ambient, and maximum loading.

Note 3: Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Note 4: These are TRI-STATE outputs internally connected to PNP inputs. Input characteristics are measured with $I_{6,7,8}$ in a state such that the TRI-STATE output is off (high-impedance).

Note 5: "Mil" = IDM2901 JM, JM/883; "Com'l" = IDM2901 JC, NC.

Note 6: Worst case I_{CC} is at minimum temperature.

Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +6.3 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

Operating Range

P/N	Temperature	V_{CC}
IDM2901A-2 JC, NC	T_A = 0°C to +70°C	4.75V to 5.25V
IDM2901A-2 JM	T_C = −55°C to +125°C	4.50V to 5.50V
IDM2901A-2 JM/883	T_C = −55°C to +125°C	4.50V to 5.50V

Standard Screening (Conforms to MIL-STD-883 for Class C parts)

Step	MIL-STD-883 Method	Conditions	Level JC, NC	Level JM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C: 24-hour 150°C	100%	100%
Temperature Cycle	1010	C: −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B: 10,000 G	100%*	100%
Fine Leak	1014	A: 5×10^{-8} atm-cc/cm^3	100%*	100%
Gross Leak	1014	C2: Fluorocarbon	100%*	100%
Electrical Test Subgroups 1 and 7 and 9	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B Parts				
Group A Sample Tests	5005	See below for definitions of subgroups		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 5
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 5

*Not applicable to IDM2901A-2 NC

Additional Screening for Class B Parts

Step	MIL-STD-883 Method	Conditions	Level JM/883
Burn-In	1015	D: 125°C, 160 hours min	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

Group A Subgroups

(as defined in MIL-STD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum rated temperature
11	Switching	Minimum rated temperature

Electrical Characteristics Over Operating Range IDM2901A-2

Symbol	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output High Voltage	V_{CC} = min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6 mA; $Y_0/Y_1/Y_2/Y_3$	2.4			V
			I_{OH} = −1.0 mA; C_{n+4}	2.4			
			I_{OH} = −800 μA; OVR/P	2.4			
			I_{OH} = −600 μA; F_3	2.4			
			I_{OH} = −600 μA; $RAM_{0,3}/Q_{0,3}$	2.4			
			I_{OH} = −1.6 mA; $\overline{G}$	2.4			

Electrical Characteristics (continued)

Symbol	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
I_{CEX}	Output Leakage Current for F = 0 Output	V_{CC} = min; V_{OH} = 5.5 V, V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output Low Voltage	V_{CC} = min; V_{IN} = V_{IH} or V_{IL}		I_{OL} = 20 mA (Com'l) $Y_0/Y_1/Y_2/Y_3$			0.5	V
				I_{OL} = 16 mA (Mil); $Y_0/Y_1/Y_2/Y_3$			0.5	
				I_{OL} = 16 mA; $\overline{G}/F$ = 0			0.5	
				I_{OL} = 10 mA; C_{n+4}			0.5	
				I_{OL} = 10 mA; OVR/$\overline{P}$			0.5	
				I_{OL} = 8 mA; $F_3/RAM_{0,3}/Q_{0,3}$			0.5	
V_{IH}	Input High Level	Guaranteed input logical high voltage for all inputs			2.0			V
V_{IL}	Input Low Level	Guaranteed input logical low voltage for all inputs					0.8	V
V_I	Input Clamp Voltage	V_{CC} = min; I_{IN} = −18 mA					−1.5	V
I_{IL}	Input Low Current	V_{CC} = max; V_{IN} = 0.5 V		Clock/$\overline{OE}/C_n$			−0.36	mA
				$A_0/A_1/A_2/A_3$			−0.36	
				$B_0/B_1/B_2/B_3$			−0.36	
				$D_0/D_1/D_2/D_3$			−0.36	
				$I_0/I_1/I_2/I_6$			−0.36	
				$I_3/I_4/I_5$			−0.36	
				I_7/I_8			−0.36	
				$RAM_{0,3}/Q_{0,3}$ (Note 4)			−0.36	
I_{IH}	Input High Current	V_{CC} = max; V_{IN} = 2.7 V		Clock/$\overline{OE}$			20	μA
				$A_0/A_1/A_2/A_3$			20	
				$B_0/B_1/B_2/B_3$			20	
				$D_0/D_1/D_2/D_3$			20	
				$I_0/I_1/I_2/I_6/I_8$			20	
				$I_3/I_4/I_5/I_7$			20	
				$RAM_{0,3}/Q_{0,3}$ (Note 4)			100	
				C_n			20	
I_I	Input High Current	V_{CC} = max; V_{IN} = 5.5 V					1.0	mA
I_{OZH}, I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = max	$Y_0/Y_1/Y_2/Y_3$	V_O = 2.4 V			50	μA
				V_O = 0.5 V			−50	
			$RAM_{0,3}/Q_{0,3}$	V_O = 2.4 V (Note 4)			100	
				V_O = 0.5 V (Note 4)			−360	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = 5.75 V; V_O = 0.5 V		$Y_0/Y_1/Y_2/Y_3/\overline{G}$	−30		−85	mA
				C_{n+4}	−30		−85	
				OVR/$\overline{P}$	−30		−85	
				F_3	−30		−85	
				$RAM_{0,3}/Q_{0,3}$	−30		−85	
I_{CC}	Power Supply Current (Note 6)	V_{CC} = max		T_A = 25°C		160	250	mA
			JC	T_A = 0°C to +70°C		160	265	
			JM	T_C = −55°C to +125°C		160	280	
				T_C = +125°C		160	190	

Note 1: For conditions shown as min or max, use the appropriate value specified under Electrical Characteristics for the applicable device type.

Note 2: Typical limits are at V_{CC} = 5.0 V, 25°C ambient, and maximum loading.

Note 3: Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Note 4: These are TRI-STATE outputs internally connected to PNP inputs. Input characteristics are measured with $I_{6,7,8}$ in a state such that the TRI-STATE output is off (high-impedance).

Note 5: "Mil" = IDM2901A-2 JM, JM/883; "Com'l" = IDM2901A-2 JC, NC.

Note 6: Worst case I_{CC} is at minimum temperature.

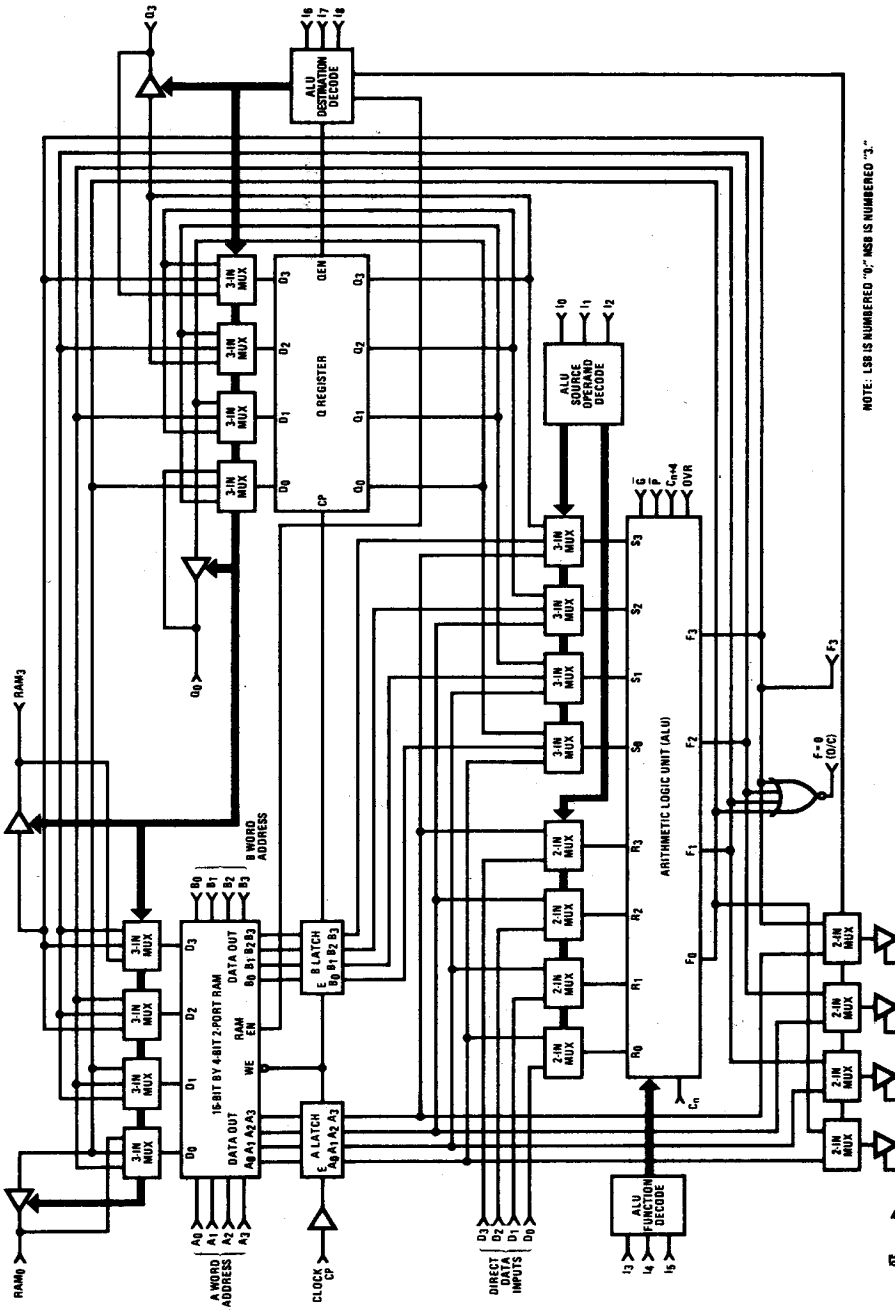
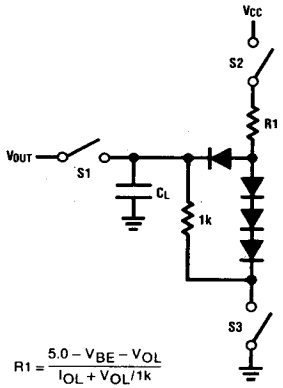


Figure 1. IDM2901 Microprocessor, Detailed Block Diagram

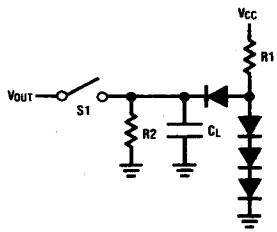
Test Output Load Configurations for IDM2901A, A-1, A-2

A. Three-State Outputs



$$R1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1k}$$

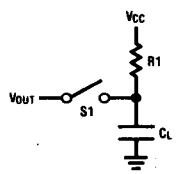
B. Normal Outputs



$$R2 = \frac{2.4V}{I_{OH}}$$

$$R1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R2}$$

C. Open-Collector Outputs



$$R1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Note 1: $C_L = 50$ pF includes scope probe, wiring and stray capacitances without device in test fixture.

Note 2: S1, S2, S3 are closed during function tests and all AC tests except output enable tests.

Note 3: S1 and S3 are closed while S2 is open for t_{PZH} test.
S1 and S2 are closed while S3 is open for t_{PZL} test.

Note 4: $C_L = 5.0$ pF for output disable tests.

TESTING CONSIDERATIONS

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400 mA in 5 ns–8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. National recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.

Test Output Loads for IDM2901A, A-1, A-2

Pin #	Pin Label	Test Circuit	R1	R2
3	RAM_3	A	560	1k
5	RAM_0	A	560	1k
7	F = 0	C	270	—
13	Q_3	A	560	1k
18	Q_0	A	560	1k
28	F_3	B	620	3.9k
29	G	B	220	1.5k
30	C_{n+4}	B	360	2.4k
31	OVR	B	470	3k
32	P	B	470	3k
33–36	Y_{0-3}	A	220	1k

Architecture

Figure 1 shows a detailed block diagram of the IDM2901. Observe that all data paths are 4 bits wide; however, the 4-bit slice can be cascaded to the number of bits required for a particular application. Although all parts of the bipolar device are important, the two key elements are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Any one of the 16 words in RAM can be read from the A-port (A_3-A_0) or the B-port (B_3-B_0); the selected word for the A-port is determined by the 4-bit A-address field, whereas the B-address field controls the output of the B-port. If the two address codes are identical, the same file data appears simultaneously at both output ports (A and B).

When enabled by RAM EN, new data is written into the file "word" defined by the B-address field; the write function is implemented when the clock input is low.

Each bit of data to be written is input via a 3-input multiplexer; this scheme permits shifting up one bit position (from LSB towards MSB), shifting down one bit position (from MSB towards LSB), or not shifting at all. A similar scheme is used when data is written into the "Q" register.

Each of the A and B data ports drives an associated 4-bit latch. These latches hold the RAM data while the clock input is low; consequently, any possibility of race conditions when writing new data is eliminated.

The high-speed ALU can perform three binary arithmetic and five logic operations on the two 4-bit input words (R_3-R_0 and S_3-S_0). The R-input field is driven from a 2-input multiplexer, whereas the S-input field is driven by a 3-input multiplexer. Both the R- and S-multiplexers have an inhibit capability, where no data is passed – this is equivalent to a "zero" source operand. Referring to figure 1, observe that the A-port output of the RAM and the 4-bit direct-data inputs (D_3-D_0) are connected to the R-input multiplexers; the S-input multiplexer has three inputs – one from the A-port of RAM, one from the B-port of RAM, and one from the Q-register.

With the foregoing input-multiplexer scheme, the inputs (A, B, D, Q, and "Zero"), when taken in pairs, provide any one of ten source operands for the ALU – AB, AD, AQ, A0, BD, BQ, B0, DQ, D0, and Q0. When the A and B address fields for RAM are identical, it is clear that certain combinations (AD/BD, AQ/BQ, and A0/B0) are redundant; that is, the identical function is implemented for either operand. Only seven of the combinations are completely nonredundant. Eight of the ten combinations (source operands) are implemented by the IDM2901A microprocessor. The ALU source operands are selected by three microinstruction inputs – I_0, I_1, and I_2. These inputs are defined in figure 2. Each of the preceding D and Q operands provides an essential function. The D input (direct-data) is used to load the working registers inside the 2901 device; also, this input source can be used to modify data files within the ALU. The Q-register is an internal 4-bit data source that is well suited for a multiply/divide operation; however, for some applications, it can be used as a data-holding register or as an accumulator.

The ALU is a high-speed arithmetic/logic operator that is capable of performing three binary arithmetic functions and five logic functions. Three microinstruction inputs (I_3, I_4, and I_5) are used to select one of the eight functions; these inputs, along with their octal codes, are defined in figure 3.

Micro Code				ALU Source Operands	
I_2	I_1	I_0	Octal Code	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	O	Q
L	H	H	3	O	B
H	L	L	4	O	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	O

Figure 2. ALU Source Operand Control

Micro Code				ALU Function	Symbol
I_5	I_4	I_3	Octal Code		
L	L	L	0	R Plus S	R + S
L	L	H	1	S Minus R	S – R
L	H	L	2	R Minus S	R – S
L	H	H	3	R OR S	R ∨ S
H	L	L	4	R AND S	R ∧ S
H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
H	H	L	6	R EX-OR S	R ∀ S
H	H	H	7	R EX-NOR S	$\overline{R \forall S}$

Figure 3. ALU Function Control

Normally, the look-ahead carry mode is used when cascading the ALUs of several microprocessor devices. The carry generate ($\overline{G}$) and carry propagate ($\overline{P}$) outputs are suitable for use in a carry-look-ahead generator. A carry-out (C_{n+4}) is also generated and is available for use as the carry flag in a status register or as a ripple-carry output. Both carry-in (C_n) and carry-out (C_{n+4}) are active-high signals. Three other status-oriented outputs are available from the ALU; these are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU, and, without enabling the TRI-STATE outputs, it can be used to determine positive or negative results. When enabled, the logic level of F_3 is identical to that of sign bit Y_3. The F = 0 output is used for zero detect; F = 0 is high when all F outputs are low. The F = 0 output is of the open-collector type and can be wire ORed between microprocessor slices. The overflow (OVR) output is used to flag arithmetic operations that exceed the available twos-complement number range. When an overflow exists (C_{n+3} and C_{n+4} are of opposite polarity), the OVR output is high.

Outputs from the ALU can be stored in the register file or the Q register, or can be transmitted to the outside world. Eight possible destination codes are defined by microinstruction inputs I_6, I_7, and I_8; the various destination control codes are shown in figure 4. The 4-bit data field (Y_3-Y_0) is a TRI-STATE output that can be directly bus organized. The Y outputs are enabled by $\overline{OE}$; when this control signal is high, the Y-outputs are TRI-STATEd. A 2-input multiplexer is also used at the Y-output port to select either the A port of RAM or the F output of the ALU; this selection is controlled by the previously described microinstruction inputs (I_6, I_7, and I_8).

As previously described, the RAM inputs (register file) are driven by a 3-input multiplexer. Thus, outputs from the ALU can be entered nonshifted, shifted up (towards MSB) one position (x 2), or shifted down (towards LSB) one position (÷ 2). The shifter is equipped with two ports — RAM_0 and RAM_3; both ports consist of a TRI-STATE buffer-driver, each of which supplies one input to the foregoing multiplexer. In the shift-up (x 2) mode, the RAM_3 output driver and the RAM_0 multiplexer input are enabled, whereas in the shift-down (÷ 2) mode, the RAM_0 output driver and RAM_3 multiplexer input are enabled; in the no-shift mode, both drivers are TRI-STATE and neither multiplexer input is enabled. The shifter is controlled by the I_6, I_7, and I_8 microinstruction inputs.

The Q register likewise is driven from a 3-input multiplexer and the Q shifter is equipped with two input/output ports — Q_0 and Q_3. Operation of these two ports is similar to that of the RAM shifter, and the ports are controlled by I_6, I_7, and I_8. In the shift-up or shift-down modes, the Q register is shifted in a specified direction with the input/output terminals of the register being an input (for a shift-up) or an output (for a shift-down). In the no-shift mode, the multiplexer may enter the ALU data into the Q register; in this case, input/output lines of the register are TRI-STATE.

The clock input shown in figure 1 controls the RAM, the A and B latches, and the Q register. When the clock input is high, the A and B latches are open and data from the RAM outputs is allowed to pass through to the ALU or "Y" outputs. When the clock input is low, both latches are closed and the last data entered is retained. When the clock input is low and if the input control code (I_6, I_7, and I_8) has enabled a file-write operation, new data, as defined by the 4-bit B-address field, is written into the RAM file. When enabled, data is clocked into the Q register on the low-to-high transition of the clock pulse.

Source Operands and ALU Functions

Any one of eight source operand pairs can be selected by instruction inputs I_0, I_1, and I_2 for use by the ALU; instruction inputs I_3, I_4, and I_5 then control function selection for the ALU — five logic and three arithmetic functions. In the arithmetic mode, the carry input (C_n) also affects the ALU functions; the carry input has no effect on the "F" result in the logic mode. These control parameters (I_6-I_0 and C_n) are summarized in figure 5 to completely define the ALU/source operand functions.

The ALU functions can also be examined on a task basis: that is, add, subtract, AND, OR, and so on. Again, in the arithmetic mode, the carry input will affect the result, whereas in the logic mode it will not. Figures 6 and 7, respectively, define the various logic and arithmetic functions of the ALU; both carry states (C_n = 0/C_n = 1) are defined in the function matrices.

Figure 4. ALU Destination Control

Micro Code				RAM Function		Q-Reg. Function		Y Output	RAM Shifter		Q Shifter	
I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
L	L	L	0	X	None	None	F → Q	F	X	X	X	X
L	L	H	1	X	None	X	None	F	X	X	X	X
L	H	L	2	None	F → B	X	None	A	X	X	X	X
L	H	H	3	None	F → B	X	None	F	X	X	X	X
H	L	L	4	Down	F/2 → B	Down	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
H	L	H	5	Down	F/2 → B	X	None	F	F_0	IN_3	Q_0	X
H	H	L	6	Up	2F → B	Up	2Q → Q	F	IN_0	F_3	IN_0	Q_3
H	H	H	7	Up	2F → B	X	None	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a TRI-STATE output which is in the high-impedance state.
B = Register Addressed by B inputs.
Up is toward MSB, Down is toward LSB.

Figure 5. Source Operand and ALU Function Matrix

Octal $I_{5,4,3}$	$I_{2,1,0}$ Octal / ALU Source / ALU Function	0 A, Q	1 A, B	2 O, Q	3 O, B	4 O, A	5 D, A	6 D, Q	7 D, O
0	C_n = L R Plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q − A − 1 Q − A	B − A − 1 B − A	Q − 1 Q	B − 1 B	A − 1 A	A − D − 1 A − D	Q − D − 1 Q − D	− D − 1 − D
2	C_n = L R Minus S C_n = H	A − Q − 1 A − Q	A − B − 1 A − B	− Q − 1 − Q	− B − 1 − B	− A − 1 − A	D − A − 1 D − A	D − Q − 1 D − Q	D − 1 D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ∀ Q	A ∀ B	Q	B	A	D ∀ A	D ∀ Q	D
7	R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR, ∧ = AND; ∀ = EX-OR.

Figure 6. ALU Logic Mode Functions (C_n Irrelevant)

Octal $I_{5,4,3}/I_{2,1,0}$	Group	Function
40	AND	A ∧ Q
41		A ∧ B
45		D ∧ A
46		D ∧ Q
30	OR	A ∨ Q
31		A ∨ B
35		D ∨ A
36		D ∨ Q
60	EX-OR	A ∀ Q
61		A ∀ B
65		D ∀ A
66		D ∀ Q
70	EX-NOR	$\overline{A \forall Q}$
71		$\overline{A \forall B}$
75		$\overline{D \forall A}$
76		$\overline{D \forall Q}$
72	INVERT	$\overline{Q}$
73		$\overline{B}$
74		$\overline{A}$
77		$\overline{D}$
62	PASS	Q
63		B
64		A
67		D
32	PASS	Q
33		B
34		A
37		D
42	"ZERO"	0
43		0
44		0
47		0
50	MASK	$\overline{A}$ ∧ Q
51		$\overline{A}$ ∧ B
55		$\overline{D}$ ∧ A
56		$\overline{D}$ ∧ Q

Figure 7. ALU Arithmetic Mode Functions

Octal $I_{5,4,3}/I_{2,1,0}$	C_n = 0 (Low)		C_n = 1 (High)	
	Group	Function	Group	Function
00	ADD	A + Q	ADD plus one	A + Q + 1
01		A + B		A + B + 1
05		D + A		D + A + 1
06		D + Q		D + Q + 1
02	PASS	Q	Increment	Q + 1
03		B		B + 1
04		A		A + 1
07		D		D + 1
12	Decrement	Q − 1	PASS	Q
13		B − 1		B
14		A − 1		A
27		D − 1		D
22	1s Comp	− Q − 1	2s Comp (Negate)	− Q
23		− B − 1		− B
24		− A − 1		− A
17		− D − 1		− D
10	Subtract (1s Comp)	Q − A − 1	Subtract (2s Comp)	Q − A
11		B − A − 1		B − A
15		A − D − 1		A − D
16		Q − D − 1		Q − D
20		A − Q − 1		A − Q
21		A − B − 1		A − B
25		D − A − 1		D − A
26		D − Q − 1		D − Q

Pinout Descriptions of IDM2901

Pin functions for the IDM2901 4-bit slice microprocessor are as follows:

$A_3 - A_0$ 4-bit address field used to select one of the file registers whose contents are displayed through the A port of RAM.

$B_3 - B_0$ 4-bit address field used to select one of the file registers whose contents are displayed through the B port of RAM. When the clock is low, new data can be written into the selected B-port register.

$I_8 - I_0$ Nine instruction-control lines — $I_0/I_1/I_2$ determine data sources of ALU, $I_3/I_4/I_5$ select ALU function, and $I_6/I_7/I_8$ select data inputs for the Q register or the register file.

Q_3/RAM_3 Serves as shift data input/output lines for the most significant bit (MSB) of Q register (Q_3) and the register stack (RAM_3). These lines are TRI-STATE outputs that connect to TTL inputs within the IDM2901 device. When the destination code, as defined by $I_6/I_7/I_8$, indicates an up-shift (octal 6 or 7), the TRI-STATE outputs are enabled; accordingly, the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, these output lines are TRI-STATE or serve as LS-TTL inputs. When a down-shift is indicated by the destination code, the Q_3 and RAM_3 pins are used as data inputs to the MSB of the Q register or RAM.

Q_0/RAM_0 These shift lines are similar to Q_3 and RAM_3, except they operate on the least significant bit (LSB) of the Q register and RAM. To transfer data for up- and down-shifts of the Q register and the ALU, the Q_0 and RAM_0 pins are connected, respectively, to the next less-significant device (Q_n and RAM_n) in the cascaded chain.

$D_3 - D_0$ A 4-bit data field that can be selected as a source of external data for ALU — D_0 is the least significant bit.

$Y_3 - Y_0$ 4-bit output data of IDM2901. These lines are TRI-STATE; when enabled, they provide either the ALU output or data from the A port of the register file — the selected source is determined by the destination code, as defined by I_6, I_7, and I_8.

$\overline{OE}$ When the Output Enable ($\overline{OE}$) signal is high, the Y outputs are inactive; when the signal is active-low, the active high or low outputs are enabled.

$\overline{P}/\overline{G}$ Carry generate and propagate outputs — see figure 8 for logic equations.

OVR The overflow flag corresponds to the exclusive-OR of the carry-in and carry-out of the MSB of the ALU. When set high, it indicates that the result of an arithmetic twos-complement operation has overflowed into the sign bit — see figure 8 for the logic equation.

$F = 0$ An open-collector output that goes high if all data lines ($F_3 - F_0$) are low, that is, the result of an ALU operation is zero.

C_n Carry-in to ALU.

C_{n+4} Carry-out of ALU — see figure 8 for logic equations.

CP Clock input. Outputs of Q register and file are clocked on low-to-high transition; the low interval of the clock input corresponds to the "write enable" period of the 16-by-4 RAM, that is, the "master" latches of the register file. When the clock is low, the output latches store the data previously held at the RAM outputs; thus, synchronous master-slave operation of the register file is permitted.

F_3 Most significant (sign) bit output of the ALU.

Logic Functions for G, P, Cn+4, and OVR

When the IDM2901 is in the add or the subtract mode, four signals (G, P, C_{n+4}, and OVR) are available to indicate carry and overflow conditions. Based on the eight ALU functions, logic equations for these signal are shown in figure 8. (Note: The "R" and "S" inputs are selected according to figure 2.)

Definitions (+ = OR):

$P_0 = R_0 + S_0$ $\quad G_0 = R_0 S_0$

$P_1 = R_1 + S_1$ $\quad G_1 = R_1 S_1$

$P_2 = R_2 + S_2$ $\quad G_2 = R_2 S_2$

$P_3 = R_3 + S_3$ $\quad G_3 = R_3 S_3$

$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$

$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

$I_{5,4,3}$	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S − R	Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions.			
2	R − S	Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions.			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R} \wedge S$	LOW	Same as $R \overline{\wedge} S$ equations, but substitute $\overline{R_i}$ for R_i in definitions.		
6	$R \forall S$	Same as $R \overline{\forall} S$ equations, but substitute $\overline{R_i}$ for R_i in definitions.			
7	$\overline{R \forall S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$	See Note 1	See Note 2

Note 1: $\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0(G_0 + \overline{C_n})}$ **Note 2:** $[\overline{P}_2 + \overline{G}_2\overline{P}_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \forall [\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$

Figure 8. Logic Equations for Flag Outputs

Guaranteed Operating Conditions Over Temperature and Voltage for IDM2901A

When operated in a system, the timing requirements for the IDM2901 are defined in tables 1, 2, and 3. Table 1 provides clock characteristics of the IDM2901, table 2 gives the combinational delay times from input to output, and table 3 specifies setup and hold times. If used according to the specified delay and setup times, the device is guaranteed to function properly over the entire operating range. Table 3 defines the time prior to the end of the cycle (low-to-high transition of clock pulse) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Table 1. Cycle Time and Clock Characteristics

Time	IDM2901A	
	JC, NC	JM, JM/883
Read-Modify-Write Cycle (time from selection of A,B registers to end of cycle)	60 ns	75 ns
Maximum Clock Frequency to Shift Q Register (50% duty cycle)	16 MHz	16 MHz
Minimum Clock Low Time	30 ns	30 ns
Minimum Clock High Time	30 ns	30 ns
Minimum Clock Period	60 ns	75 ns

Table 2. Maximum Combinational Propagation Delays (all in ns; $C_L \leq 50$ pF)

	Commercial IDM2901A JC, NC (0°C to +70°C; 5V ± 5%)								Military IDM2901A JM, JM/883 (−55°C to +125°C; 5V ± 10%)							
To Output / From Input	Y	F_3	C_{n+4}	$\overline{G}/\overline{P}$	F=0 R_L = 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3	Y	F_3	C_{n+4}	$\overline{G}/\overline{P}$	F=0 R_L = 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3
A, B	65	65	65	60	70	65	70	–	80	80	80	65	85	80	80	–
D (arithmetic mode)	40	40	40	35	55	45	50	–	45	45	45	40	65	55	60	–
D (I = X37)	40	40	–	–	55	–	50	–	45	45	–	–	60	–	60	–
C_n	30	30	20	–	40	30	35	–	35	35	25	–	50	35	45	–
$I_{2,1,0}$	55	50	50	45	60	50	60	–	60	60	55	50	75	60	75	–
$I_{5,4,3}$	50	50	50	45	55	50	50	–	60	60	60	55	70	60	60	–
$I_{8,7,6}$	30	–	–	–	–	–	30	30	35	–	–	–	–	–	35	35
$\overline{OE}$ Enable/Disable	30/25	–	–	–	–	–	–	–	40/25	–	–	–	–	–	–	–
A Bypassing ALU (I = 2xx)	40	–	–	–	–	–	–	–	50	–	–	–	–	–	–	–
Clock ↓ (Note 6)	60	60	60	50	60	55	60	30	65	65	65	55	75	70	75	35

Table 3. Maximum Setup and Hold Times (all in ns) — Note 1

		Commercial IDM2901A JC, NC (0°C to +70°C, 5V ± 5%)		Military IDM2901A JM, JM/883 (−55°C to +125°C, 5V ± 10%)	
From Input	Notes	Setup Time	Hold Time	Setup Time	Hold Time
A, B Source	2, 3, 4, 5	60, $t_{pw}L$ + 20	0	75, $t_{pw}L$ + 25	0
B Destination	2, 4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
D (arithmetic mode)		40	0	50	0
D (I = X37)	5	40	0	50	0
C_n		35	0	40	0
$I_{2,1,0}$		45	0	55	0
$I_{5,4,3}$		45	0	55	0
$I_{8,7,6}$	4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
$RAM_{0,3}/Q_{0,3}$		20	0	25	0

Note 1: See figures 9 and 10.

Note 2: If the B address is used as a source operand, allow for the "A, B Source" setup time; if it is used only for the destination address, use the "B Destination" setup time.

Note 3: Where two numbers are shown, both must be met.

Note 4: "$t_{pw}L$" is the clock low time.

Note 5: DVO is the fastest way to load the RAM from the D inputs. This function is obtained with I = X37.

Note 6: Using Q register as source operand in arithmetic mode. Clock is not normally in critical speed path when Q is not a source.

Guaranteed Operating Conditions Over Temperature and Voltage for IDM2901A-1

When operated in a system, the timing requirements for the IDM2901A-1 are defined in tables 1, 2, and 3. Table 1 provides clock characteristics of the IDM2901A-1, table 2 gives the combinational delay times from input to output, and table 3 specifies setup and hold times. If used according to the specified delay and setup times, the device is guaranteed to function properly over the entire operating range. Table 3 defines the time prior to the end of the cycle (low-to-high transition of clock pulse) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Table 1. Cycle Time and Clock Characteristics

Time	IDM2901A-1	
	JC, NC	JM, JM/883
Read-Modify-Write Cycle (time from selection of A, B registers to end of cycle)	60 ns	75 ns
Maximum Clock Frequency to Shift Q Register (50% duty cycle)	16 MHz	16 MHz
Minimum Clock Low Time	30 ns	30 ns
Minimum Clock High Time	30 ns	30 ns
Minimum Clock Period	60 ns	75 ns

Table 2. Maximum Combinational Propagation Delays (all in ns; $C_L \leq 50$ pF)

	Commercial IDM2901A-1 JC, NC (0°C to +70°C; 5V ± 5%)								Military IDM2901A-1 JM, JM/883 (−55°C to +125°C; 5V ± 10%)							
To Output / From Input	Y	F_3	C_{n+4}	$\overline{G}/\overline{P}$	F=0 R_L = 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3	Y	F_3	C_{n+4}	$\overline{G}/\overline{P}$	F=0 R_L = 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3
A, B	50	50	50	45	55	60	55	–	60	60	60	60	65	75	65	–
D (arithmetic mode)	32	32	32	30	32	40	35	–	40	40	40	40	40	50	45	–
D (I = X37)	32	32	–	–	32	–	35	–	40	40	–	–	40	–	45	–
C_n	25	22	16	–	30	25	35	–	32	30	20	–	40	35	45	–
$I_{2,1,0}$	40	35	35	30	40	45	45	–	50	45	45	40	50	55	55	–
$I_{5,4,3}$	35	35	35	32	40	45	45	–	45	45	45	40	50	55	55	–
$I_{8,7,6}$	25	–	–	–	–	–	30	30	35	–	–	–	–	–	35	35
$\overline{OE}$ Enable/Disable	20/20	–	–	–	–	–	–	–	25/25	–	–	–	–	–	–	–
A Bypassing ALU (I = 2xx)	40	–	–	–	–	–	–	–	50	–	–	–	–	–	–	–
Clock ↓ (Note 6)	50	45	45	40	50	55	55	30	60	55	55	50	60	65	65	35

Table 3. Maximum Setup and Hold Times (all in ns) — Note 1

		Commercial IDM2901A-1 JC, NC (0°C to +70°C, 5V ± 5%)		Military IDM2901A-1 JM, JM/883 (−55°C to +125°C, 5V ± 10%)	
From Input	Notes	Setup Time	Hold Time	Setup Time	Hold Time
A, B Source	2, 3, 4, 5	60, $t_{pw}L$ + 20	0	75, $t_{pw}L$ + 25	0
B Destination	2, 4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
D (arithmetic mode)		40	0	50	0
D (I = X37)	5	40	0	50	0
C_n		35	0	40	0
$I_{2,1,0}$		45	0	55	0
$I_{5,4,3}$		45	0	55	0
$I_{8,7,6}$	4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
$RAM_{0,3}/Q_{0,3}$		15/10	0	25/15	0

Note 1: See figures 9 and 10.
Note 2: If the B address is used as a source operand, allow for the "A, B Source" setup time; if it is used only for the destination address, use the "B Destination" setup time.
Note 3: Where two numbers are shown, both must be met.
Note 4: "$t_{pw}L$" is the clock low time.
Note 5: DVO is the fastest way to load the RAM from the D inputs. This function is obtained with I = X37.
Note 6: Using Q register as source operand in arithmetic mode. Clock is not normally in critical speed path when Q is not a source.

Guaranteed Operating Conditions Over Temperature and Voltage for IDM2901A-2

When operated in a system, the timing requirements for the IDM2901A-2 are defined in tables 1, 2, and 3. Table 1 provides clock characteristics of the IDM2901A-2, table 2 gives the combinational delay times from input to output, and table 3 specifies setup and hold times. If used according to the specified delay and setup times, the device is guaranteed to function properly over the entire operating range. Table 3 defines the time prior to the end of the cycle (low-to-high transition of clock pulse) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

TABLE 1. Cycle Time and Clock Characteristics

Time	IDM2901A-2	
	JC, NC	JM, JM/883
Read-Modify-Write Cycle (time from selection of A, B registers to end of cycle)	50 ns	65 ns
Maximum Clock Frequency to Shift Q Register (50% duty cycle)	20 MHz	16 MHz
Minimum Clock Low Time	25 ns	30 ns
Minimum Clock High Time	25 ns	30 ns
Minimum Clock Period	50 ns	65 ns

TABLE 2. Maximum Combinational Propagation Delays (all in ns; C_L 50pF)

	Commercial IDM2901A-2 JC, NC (0°C to +70°C; 5V ± 5%)								Military IDM2901A-2 JM, JM/883 (−55°C to +125°C; 5V ± 10%)							
to Output / from Input	Y	F_3	C_{n+4}	G/P	F=0 R_L = 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3	Y	F_3	C_{n+4}	G/P	F=0 R_L = 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3
A, B	44	44	44	35	44	45	40	–	55	50	50	45	55	55	50	–
D (arithmetic mode)	28	28	28	25	31	34	30	–	37	37	37	34	40	40	37	–
D (I = X37)	28	28	–	–	31	–	30	–	37	37	–	–	40	–	37	–
C_n	25	22	16	–	25	25	25	–	30	25	19	–	33	30	30	–
$I_{2,1,0}$	35	35	35	28	35	39	35	–	45	45	45	45	45	45	40	–
$I_{5,4,3}$	35	35	35	32	35	35	35	–	45	40	40	40	45	45	40	–
$I_{8,7,6}$	25	–	–	–	–	–	30	30	30	–	–	–	–	–	35	35
OE Enable/Disable	20/20	–	–	–	–	–	–	–	25/25	–	–	–	–	–	–	–
A Bypassing ALU (I = 2xx)	35	–	–	–	–	–	–	–	45	–	–	–	–	–	–	–
Clock (Note 6)	40	40	40	40	40	45	45	28	50	45	45	40	55	50	50	30

TABLE 3. Maximum Setup and Hold Times (all in ns) — Note 1

		Commercial IDM2901A-2 JC, NC (0°C to +70°C, 5V ± 5%)		Military IDM2901A-2 JM, JM/883 (−55°C to +125°C, 5V ± 10%)	
From Input	Notes	Setup Time	Hold Time	Setup Time	Hold Time
A, B Source	2, 3, 4, 5	50, $t_{pw}L$ + 20	0	60, $t_{pw}L$ + 20	0
B Destination	2, 4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
D (arithmetic mode)		35	0	40	0
D (I = X37)	5	35	0	40	0
C_n		26	0	30	0
$I_{2,1,0}$		35	0	45	0
$I_{5,4,3}$		30	0	45	0
$I_{8,7,6}$	4	$t_{pw}L$ + 10	0	$t_{pw}L$ + 14	0
$RAM_{0,3}/Q_{0,3}$		12/10	0	15/15	0

Note 1: See figures 9 and 10.

Note 2: If the B address is used as a source operand, allow for the "A, B Source" setup time; if it is used only for the destination address, use the "B Destination" setup time.

Note 3: Where two numbers are shown, both must be met.

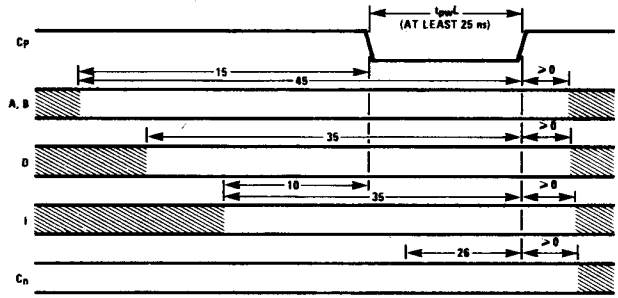
Note 4: "$t_{pw}L$" is the clock low-time.

Note 5: DVO is the fastest way to load the RAM from the D inputs. This function is obtained with I = X37.

Note 6: Using Q register as source operand in arithmetic mode. Clock is not normally in critical speed path when Q is not a source.

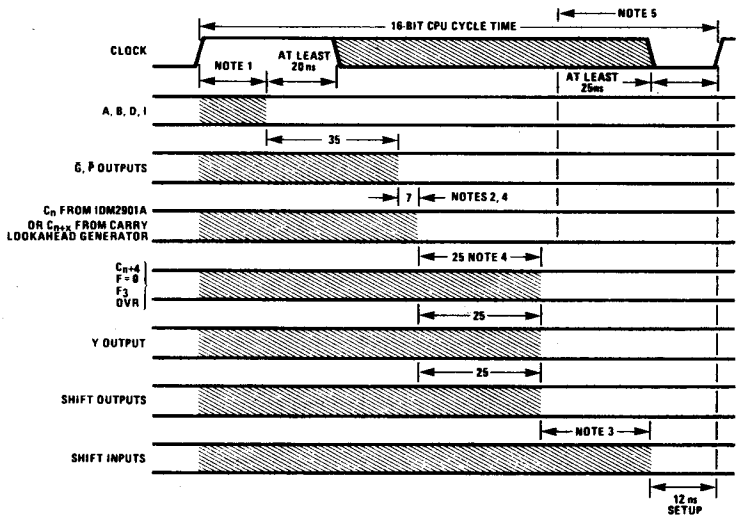
Set-Up and Hold Times (mimimum cycles from each input)

Setup and hold times are defined relative to the low-to-high transition of the clock pulse. At all times, inputs must be stable from the setup time prior to the clock until the hold time after the clock – observe that all hold times are "zero." The set-up times allow sufficient time to perform the correct operation on the correct data so that the correct ALU data can be written into the correct register.



Note: Numbers shown are minimum data-stable times in nanoseconds for commercial product – see table 3 for detailed information.

Figure 9. Setup Times for Input Parameters of IDM2901



Notes:

1. This delay is the max t_{pd} of the register containing A, B, D, and I.
2. 7 ns for look-ahead carry. For ripple carry over 16 bits use 2 x ($C_n \rightarrow C_{n+4}$), or 24 ns.
3. This is the delay associated with the multiplexer between the shift outputs and the shift inputs on the IDM2901.
4. Not applicable for logic operations.
5. Clock rising edge may occur here if add and shift do not occur on same cycle.

Figure 10. Switching Waveforms for 16-Bit System Assuming A, B, D, and I are Driven from Registers with the Same Propagation Delay and Clocked by the IDM2901. (These are maximum times in nanoseconds using commercial product specifications.)

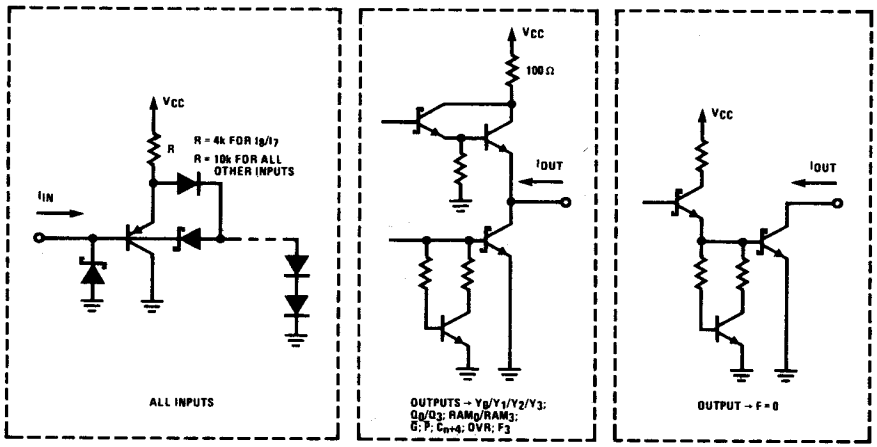


Figure 11. Equivalent Input/Output Current Interface Conditions for IDM2901

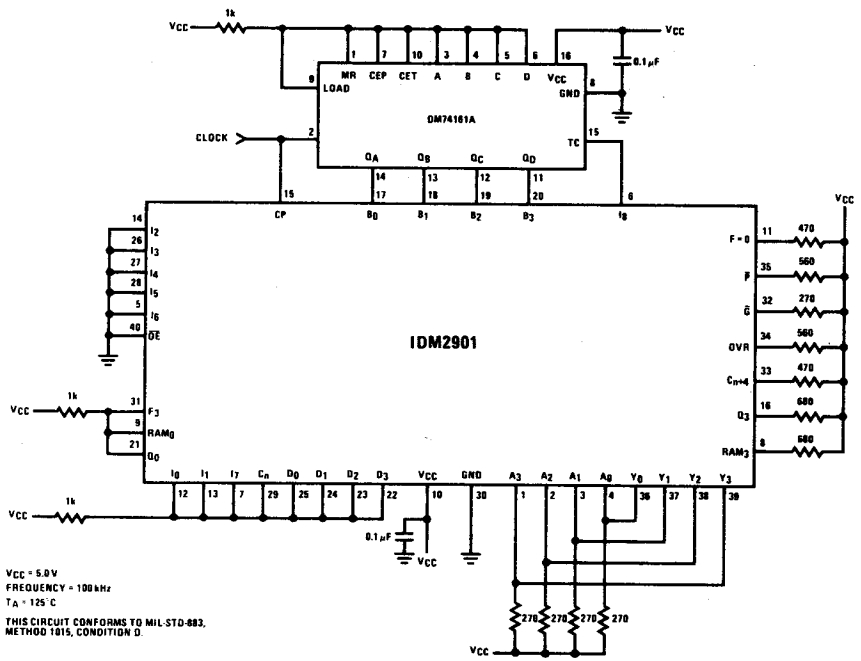
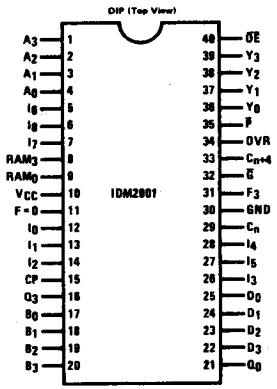


Figure 12. Burn-In Circuit for IDM2901

Connection Diagram



NOTE: PIN 1 IS MARKED FOR ORIENTATION.

Ordering Information

Package Type	Package Number	Temperature Range	Order Number
Molded DIP	N40A	0°C to +70°C	IDM2901ANC/IDM2901A-1NC/IDM2901A-2NC
Hermetic DIP	D40C	0°C to +70°C	IDM2901AJC/IDM2901A-1JC/IDM2901A-2JC
Hermetic DIP	D40C	−55°C to +125°C	IDM2901AJM/IDM2901A-1JM/IDM2901A-2JM
Hermetic DIP	D40C	−55°C to +125°C	IDM2901AJM/883/IDM2901A-1JM/883/IDM2901A-2JM/883