LSI/CSI

LS7063

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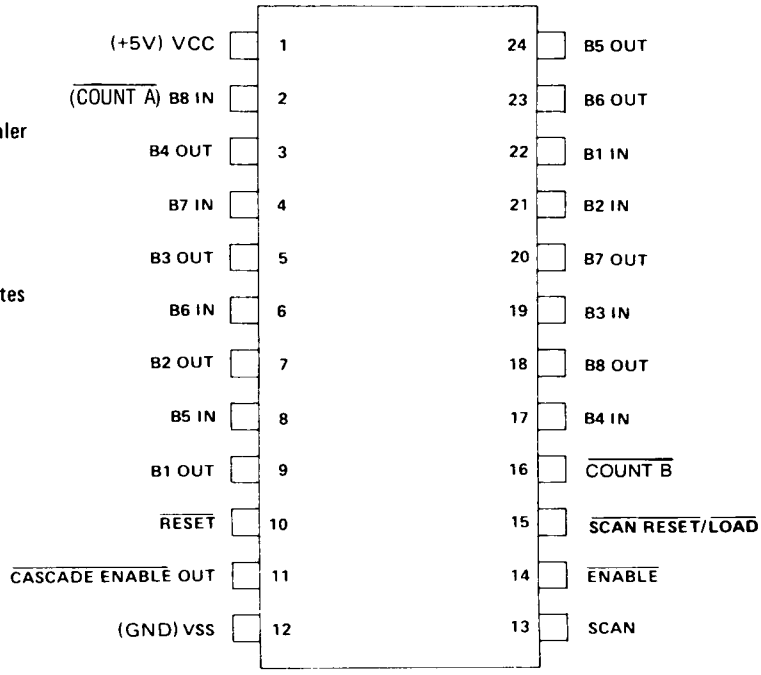
DUAL 16 BIT BINARY UP COUNTER
with 40 Bit Latch, Multiplexer and Three-State Drivers

FEATURES:

- DC to 15 MHz Count Frequency
- 8 Bit Byte Multiplexer
- DC to 1MHz Scan Frequency
- Ability to Latch External 8 Bits of High Speed External Prescaler Thereby Extending Count Frequency to 3.84 GHz
- Single Power Supply Operation, +4.75 VDC to +5.25 VDC
- Three-State Data Outputs, Bus and TTL Compatible
- Inputs TTL, NMOS and CMOS Compatible
- Unique Cascade Feature Allows Multiplexing of Successive Bytes of Data in Sequence in Multiple Counter Systems
- Low Power Dissipation
- All Inputs Protected
- 24 Pin DIP



TOP VIEW
LS7063 PIN ASSIGNMENT
Figure 1

DESCRIPTION:

The LS7063 is a monolithic, ion implanted MOS Silicon Gate, dual 16 bit up counter. The circuit includes 40 latches, multiplexer, eight three-state binary data output drivers and output cascading logic.

DESCRIPTION OF OPERATION:

16 BIT BINARY UP COUNTER

The 16 bit static ripple through counter increments on the negative edge of the input count pulse.
Maximum ripple time is 2μs (transition count of sixteen "ones" to sixteen "zeros").
Guaranteed count frequency is DC to 15 MHz.

B8 (COUNT A)

Input count pulses to the first 16 bit counter are applied through this input. This input is the most significant bit of the external data byte.

RESET

All 16 counter bits are reset to zero when Reset is brought low for a minimum of 1μs. Reset must be high for a minimum of 300ns before next valid count can be recorded. Count B must be held low when reset is brought low to ensure proper reset of Counter B.

$\overline{\text{COUNT B}}$

Count pulses may be applied to the last 16 bits of the binary counter through this input. The counter advances on the negative transition of these pulses.

LATCHES

40 bits of latch are provided, eight for storage of the contents of a high speed external prescaling countr and the remaining 32 for the contents of the counter data. All latches are loaded when the $\overline{\text{Load}}$ input is brought low for a minimum of 1 μs and kept low until a minimum of 2 μs has elapsed from previous negative edge of count pulse (ripple time).
Storage of valid data occurs when $\overline{\text{Load}}$ is brought high for a minimum of 250ns before next negative edge of count pulse or $\overline{\text{Reset}}$.

SCAN COUNTER AND DECODER

The scan counter is reset to the least significant byte position (State 1) when $\overline{\text{Scan Reset}}$ input is brought low for a minimum of 1 μs. The scan counter is enabled for counting as long as the $\overline{\text{Enable}}$ input is held low. The counter advances to the next significant byte position on each negative transition of the Scan pulse. When the scan counter advances to state 6 it disables the Output Drivers and stops in that state until $\overline{\text{Scan Reset}}$ is again brought low.

SCAN

When the scan counter is enabled, each negative transition of this input advances the scan counter to its next state. When Scan is low the Data Outputs are disabled. When Scan is brought high the Data Outputs are enabled and present the latched counter data corresponding to the present state of the scan counter. Therefore, in microprocessor applications, the Data Output Bus may be utilized for other activities while new data is propagating to the outputs. This positive Scan pulse can be viewed as a "Place the next byte on my bus" instruction from the microprocessor. Minimum positive and negative pulse widths of 500ns for the Scan signal are required for scan counter operation.

$\overline{\text{SCAN RESET}}/\overline{\text{LOAD}}$

When this input is brought low for a minimum of 1μs the scan counter is reset to state 1, least significant byte position, and the latches are simultaneously loaded with new count information.

$\overline{\text{ENABLE}}$

When this input is high, the scan counter and the Data Outputs are disabled. When $\overline{\text{Enable}}$ is low, the scan counter and Data Outputs are enabled for normal operation. Transition of this input should only be made while the Scan input is in a low state in order to prevent false clocking of the scan counter.

CASCADE ENABLE:

This output is normally high. It transitions low and stays low when the scan counter advances to state 6. In a multiple counter system this output is connected to the $\overline{\text{Enable}}$ input of the next counter in the cascade string. The Scan input and $\overline{\text{Scan Reset}}/\overline{\text{Load}}$ input are carried to all the counters in the "Cascade". Counter 1 then presents its bytes of data to the Output Bus on each positive transition of the Scan pulse as previously discussed. When state 6 of counter 1 is achieved, counter 2 presents its data to the output bus. This sequence continues until all counters in the cascade have been addressed. See Fig. 4 for an illustration of a 3 device cascade design. This output is TTL, CMOS and NMOS compatible.

THREE-STATE DATA OUTPUT DRIVERS:

The eight Data Output Drivers are disabled when either $\overline{\text{Enable}}$ input is high, the scan counter is in state 6, or the Scan input is low.
The Output Drivers are TTL and Bus compatible.

MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
Storage Temperature	T_{STG}	−55 to +150	°C
Operating Temperature	T_A	0 to +70	°C
Voltage(any pin to VSS)	Vmax	+10 to −0.3	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} =+5V±5%, V_{SS} = 0V, T_A=0°C to +70°C unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Units	Conditions
Power Supply Current	I_{DD}		15	mA	@Maximum Operating Frequency, V_{CC}= Max, Outputs No Load
Input High Voltage	V_{IH}	+3.5	V_{CC}	V	
Input Low Voltage	V_{IL}	0	+0.6	V	
OUTPUT HIGH VOLTAGE					
$\overline{\text{Cascade Enable}}$	V_{OH}	V_{CC}−0.2		V	I_O=0, V_{CC}=MIN.
		+2.4		V	I_O=−100μA, V_{CC}=MIN.
B1 – B8		+2.4		V	I_O= −260μA, V_{CC}=MIN.
		+2.0		V	I_O= −750μA, V_{CC}=MIN.
OUTPUT LOW VOLTAGE					
$\overline{\text{Cascade Enable}}$	V_{OL}		+0.2	V	I_O=0, V_{CC}=MIN.
			+0.4	V	I_O= 1.6mA, V_{CC}=MIN.
B1 – B8			+0.4	V	I_O= 1.6mA, V_{CC}=MIN.
Output Source Current	Isource	3.0		mA	Vo=+1.2V, V_{CC}=MIN.
B1 – B8 Outputs		4.8		mA	Vo=+0.8V, V_{CC}=MIN.
		7.3		mA	Vo=+0.4V, V_{CC}=MIN.
Output Sink Current	Isink	5.7		mA	Vo=+1.2V, V_{CC}=MIN.
B1 –B8 Outputs		4.0		mA	Vo=+0.8V, V_{CC}=MIN.
		2.2		mA	Vo=+0.4V, V_{CC}=MIN.
Output Leakage Current B1 – B8 (Off State)	I_{OL}		1	μA	Vo=+.4V to +2.4V V_{CC}=MIN.
Input Capacitance	C_{IN}		6	pF	T_A=25°C, f=1.0MHz
Output Capacitance	C_{OUT}		12	pF	T_A=25°C, f=1.0MHz
Input Leakage Current	I_{LI}		1	μA	$\overline{\text{ENABLE}}$, $\overline{\text{RESET}}$, $\overline{\text{SCAN}}$ V_{CC}=MAX
INPUT CURRENT					
*$\overline{\text{Scan Reset}}/\overline{\text{Load}}$	I_{IH}		−2.5	μA	V_{CC}=MAX, V_{IH}=+3.5
	I_{IL}		−5	μA	V_{CC}=MAX, V_{IL}=0
**B1 - B8 Inputs	I_{IH}		5	μA	V_{CC}=MAX, V_{IH}=+3.5
$\overline{\text{COUNT B}}$	I_{IL}		1	μA	V_{CC}=MAX, V_{IL}=0

*Input has internal pull-up resistor to V_{CC}
**Inputs have internal pull-down resistor to V_{SS}

DYNAMIC ELECTRICAL CHARACTERISTICS

(V_{CC}=+5V±5%, V_{SS}=0V, T_A=0°C to +70°C unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Units	Conditions
Count Frequency B8($\overline{\text{COUNT A}}$), $\overline{\text{COUNT B}}$	fc	DC	15	MHz	
Count Pulse Width B8($\overline{\text{COUNT A}}$), $\overline{\text{COUNT B}}$	t_{CPW}	30		ns	Measured @ 50% point, Max t_r, t_f =10ns
Count Rise & Fall Time B8($\overline{\text{COUNT A}}$), $\overline{\text{COUNT B}}$	t_r, t_f		30	μs	
Count Ripple Time B8($\overline{\text{COUNT A}}$), $\overline{\text{COUNT B}}$	t_{CR}		2	μs	Transition from 16 ones to 16 zeros from negative edge of count pulse
$\overline{\text{Reset}}$ Pulse Width (All Counter Stages Fully Reset)	t_{RPW}	500		ns	Measured @ 50% point Max t_r, t_f =200ns
$\overline{\text{Reset}}$ Removal Time ($\overline{\text{Reset}}$ Removed From All Counter Stages)	t_{RR}		250	ns	Measured from $\overline{\text{Reset}}$ signal @ V_{IH}
Scan Frequency	f_{sc}		1	MHz	
Scan Pulse Width	t_{SCPW}	500		ns	Measured @ 50% point Max t_r, t_f =100ns
$\overline{\text{Scan Reset}}$/$\overline{\text{Load}}$ Pulse Width (All latches loaded and Scan Counter Reset to Least Significant Byte)	t_{RSCPW}	1		μs	Measured @ 50% point Max t_r, t_f =200ns
$\overline{\text{Scan Reset}}$/$\overline{\text{Load}}$ Removal Time (Reset Removed from Scan Counter; Load Command Removed From Latches)	t_{RSCR}		250	ns	Measured from $\overline{\text{Scan Reset}}$/$\overline{\text{Load}}$ @ V_{IH}
Output Disable Delay Time (B1 – B8)	t_{DOD}		200	ns	Transition to Output High Impedance State Measured From Scan @ V_{IL} or $\overline{\text{Enable}}$ @ V_{IH}
Output Enable Delay Time (B1 – B8)	t_{DOE}		200	ns	Transition to Valid On State Measured from Scan @ V_{IH} and $\overline{\text{Enable}}$ @ V_{IL} ; Delay to Valid Data Levels for C_{OL}=10pf and one TTL Load or Valid Data Currents for High Capacitance Loads
Output Delay Time $\overline{\text{Cascade Enable}}$	t_{DCE}		300	ns	Negative Transition from Scan @V_{IL} and ST6 of Scan Counter or Positive Transition From $\overline{\text{Scan Reset}}$/$\overline{\text{Load}}$ @ V_{IL} to Valid Data Levels for C_{OL}=10pf and one TTL Load

Refer to timing diagrams.

SCAN COUNTER & DECODER OUTPUTS TIMING DIAGRAM

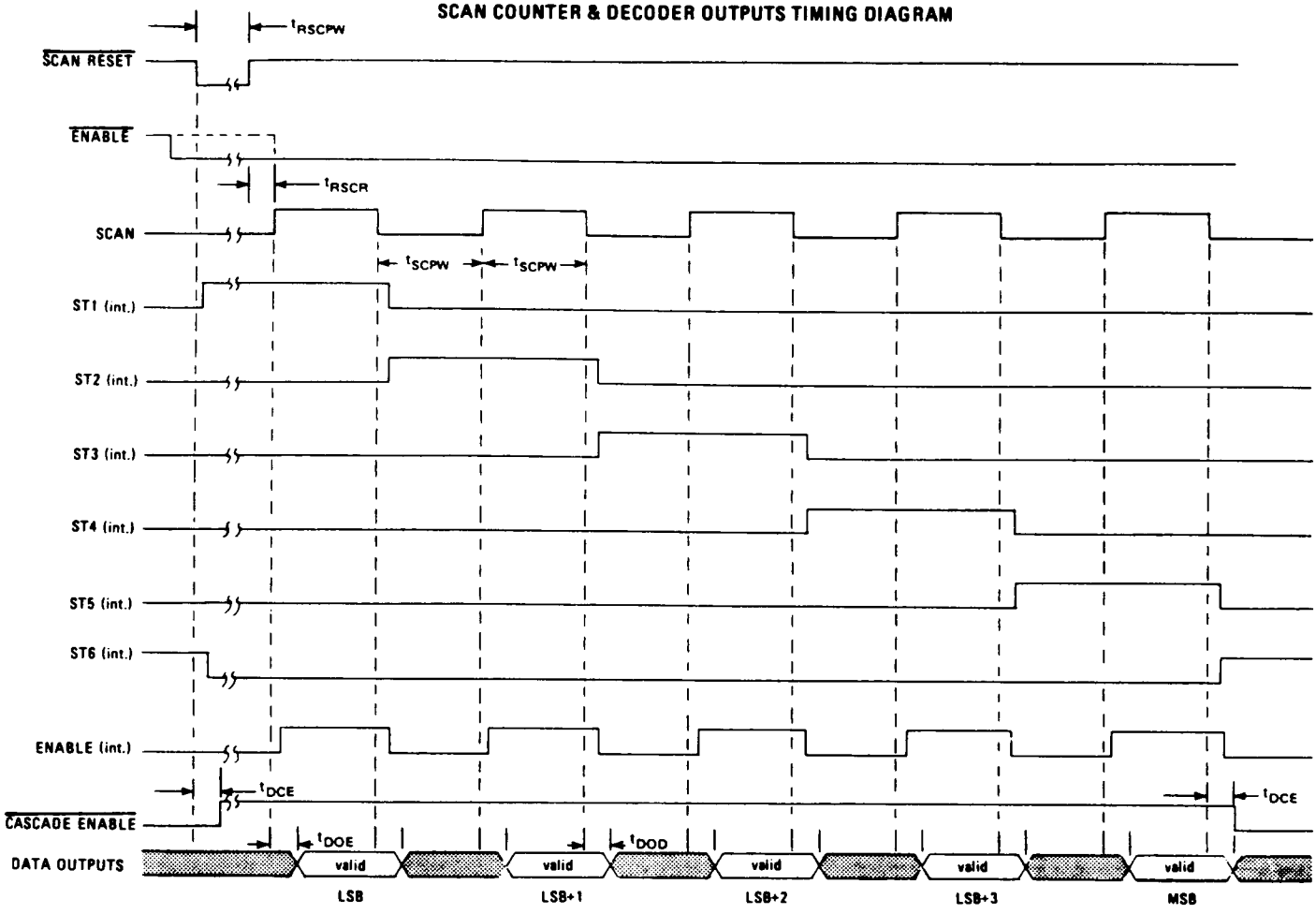


Figure 2

COUNTER TIMING DIAGRAM

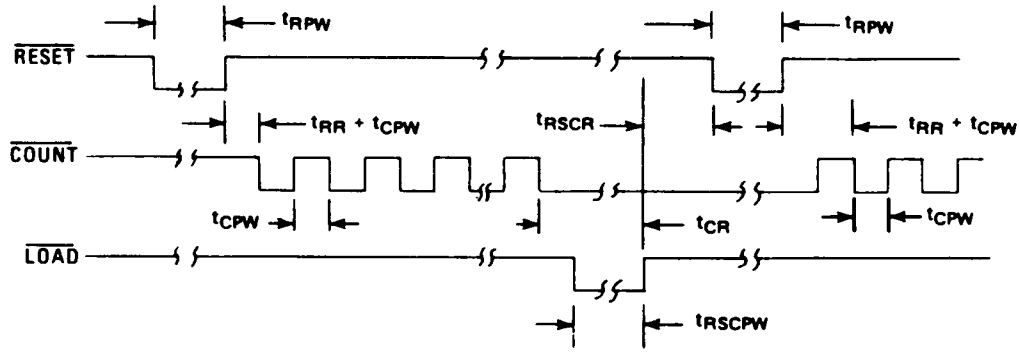


Figure 3

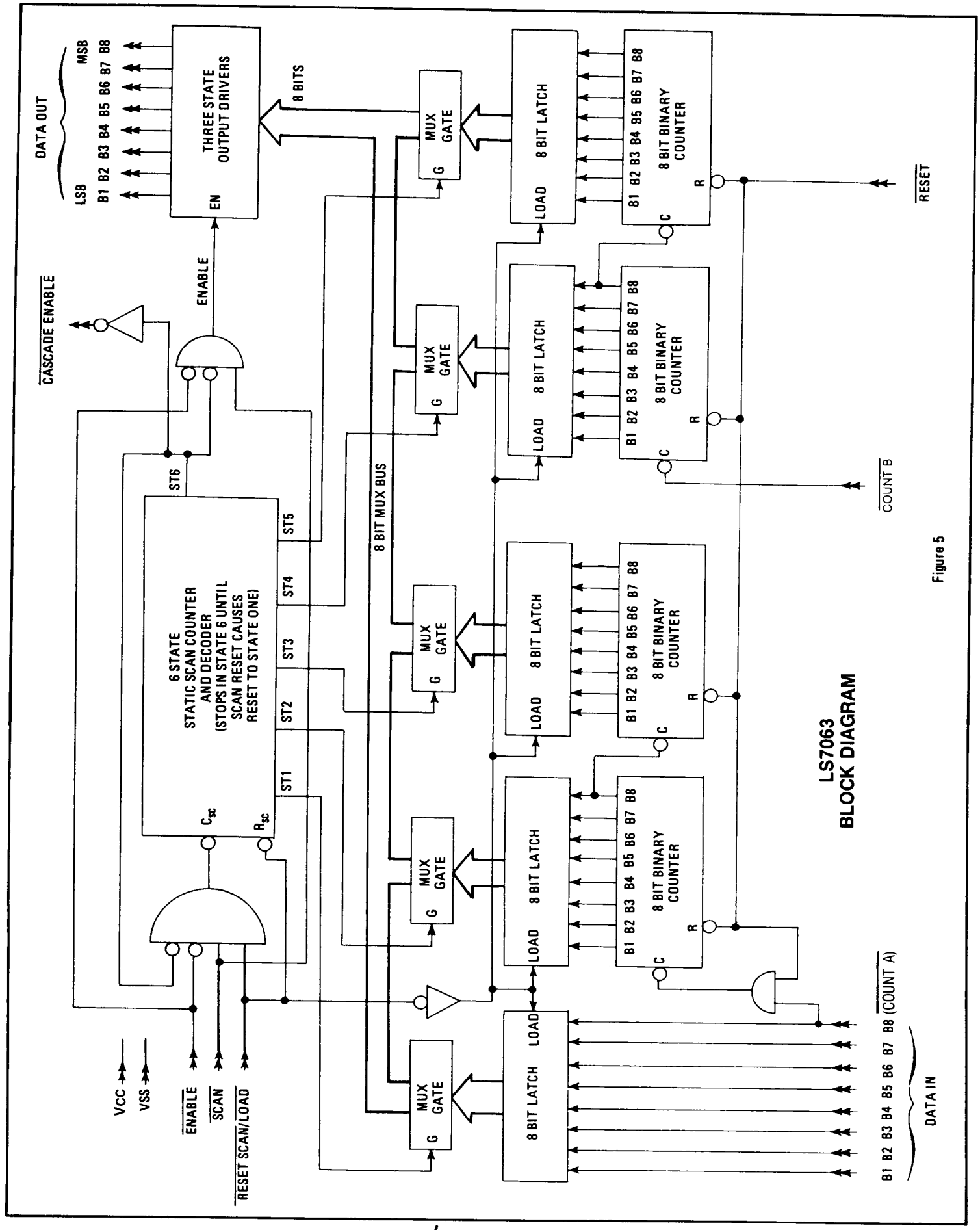
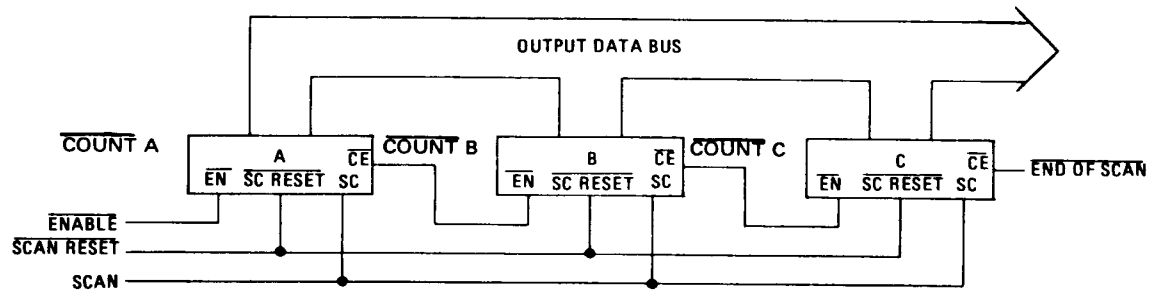


Figure 5

ILLUSTRATION OF A 3 DEVICE CASCADE



TIMING DIAGRAM

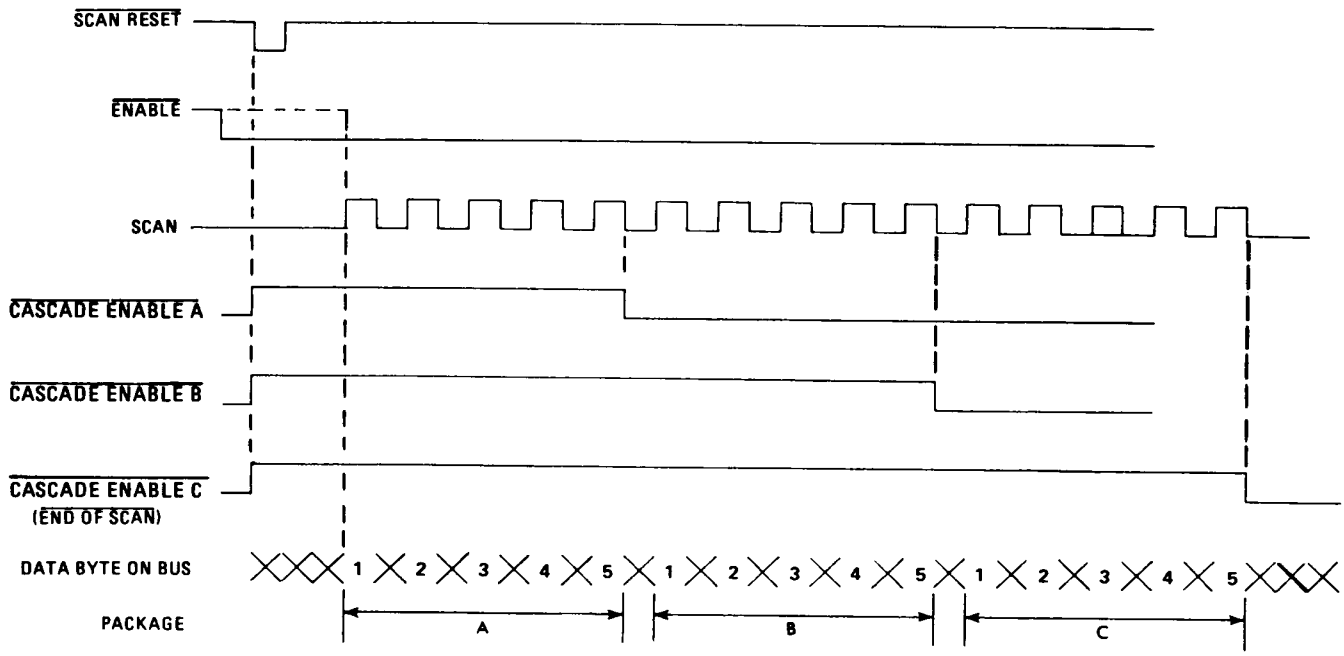
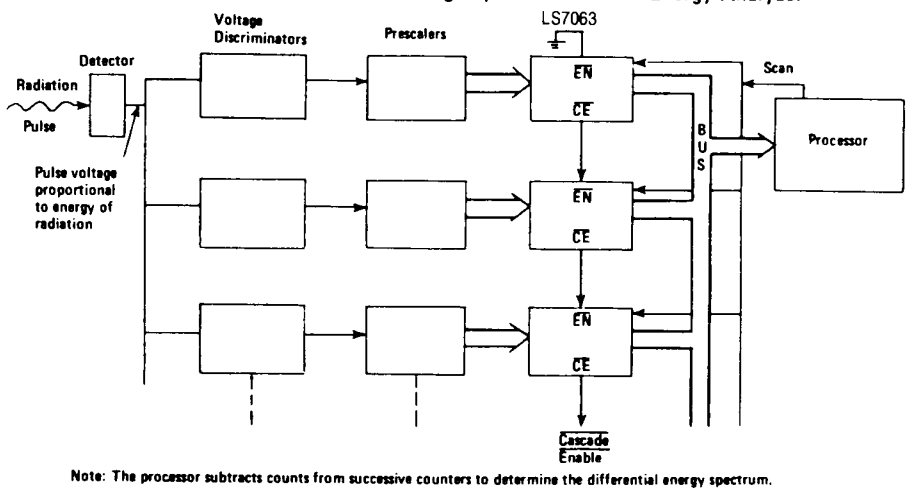


Figure 4

APPLICATION EXAMPLE: High Speed Differential Energy Analyzer



Note: The processor subtracts counts from successive counters to determine the differential energy spectrum.

Figure 6