M37102M8-XXXSP/FP, M37102E8-XXXSP/FP, M37102E8SP/FP
M37201M6-XXXSP/FP, M37201E6-XXXSP/FP, M37201E6SP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

DESCRIPTION

The M37102M8-XXXSP/FP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or an 80-pin plastic molded QFP. This single-chip microcomputer is useful for the high-tech channel selection system for TVs.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The features of the M37102E8-XXXSP/FP and the M37102ESP/FP are similar to those of the M37102M8-XXXSP/FP except that these chips have a built-in PROM which can be written electrically.

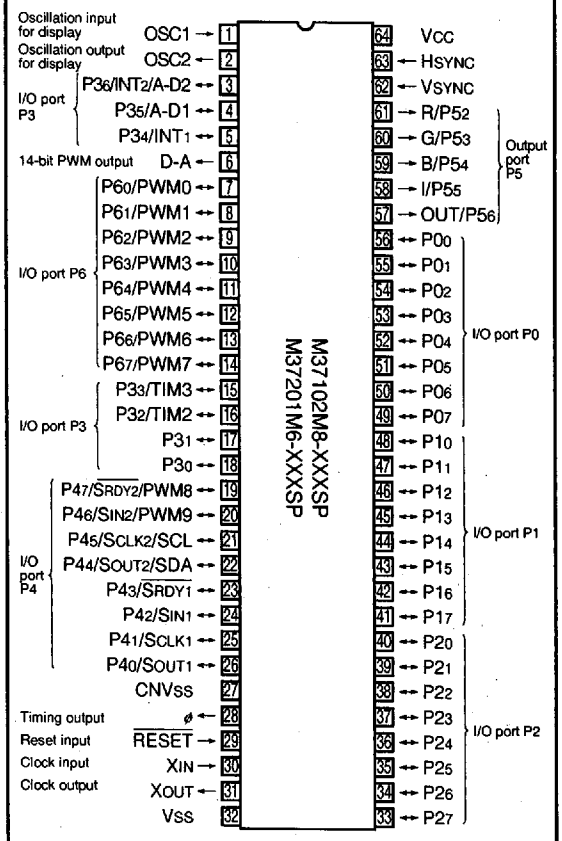
The differences between the M37102M8-XXXSP/FP and the M37201M6-XXXSP/FP are the ROM size and the RAM size as shown below. Accordingly, the following descriptions will be for the M37102M8-XXXSP/FP unless otherwise noted.

Type name	ROM size	RAM size
M37102M8-XXXSP/FP	16 K bytes	320 bytes
M37201M6-XXXSP/FP	24 K bytes	384 bytes

FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 16 K bytes (M37102M8-XXXSP/FP)
  24 K bytes (M37201M6-XXXSP/FP)
  RAM ..... 320 bytes (M37102M8-XXXSP/FP)
  384 bytes (M37201M6-XXXSP/FP)
  ROM for display ..... 4 K bytes
  RAM for display ..... 144 bytes
- The minimum instruction execution time ..... 1 μs (at 4MHz oscillation frequency)
- Power source voltage ..... 5V±10%
- Power dissipation ..... 110mW (at 4MHz oscillation frequency, V_{CC}=5.5V, at CRT display, at PLL operating)
- Subroutine nesting ..... 96 levels (Max.)
- Interrupts ..... 13 types, 13 vectors
- 8-bit timers 4
- Programmable I/O ports (Ports P0, P1, P2, P3, P4, P6) 47
- Output port (Port P5) 5
- 12 V withstand ports 10
- LED drive ports 4
- Serial I/O ..... 8-bit × 2 channel
- PWM output circuit ..... 14-bit × 1, 8-bit × 10
- A-D comparator (4-bit resolution) ..... 2 channels
- CRT display function
  - Display characters ..... 24 characters × 3 lines (16 lines max.)
  - Character kinds ..... 126 kinds
  - Dot structure ..... 12 × 16 dots
  - Character size ..... 4 kinds
  - Character color kinds (It can be specified by the character) max. 15 kinds (R, G, B, I)
  - 1/2-character unit color specification is possible
  - Raster color (max. 15 kinds)
  - Display layout
    - Horizontal ..... 64 levels
    - Vertical ..... 128 levels
  - Bordering (horizontal and vertical)
  - Wipe function
  - Scanning line double count mode display is possible.

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

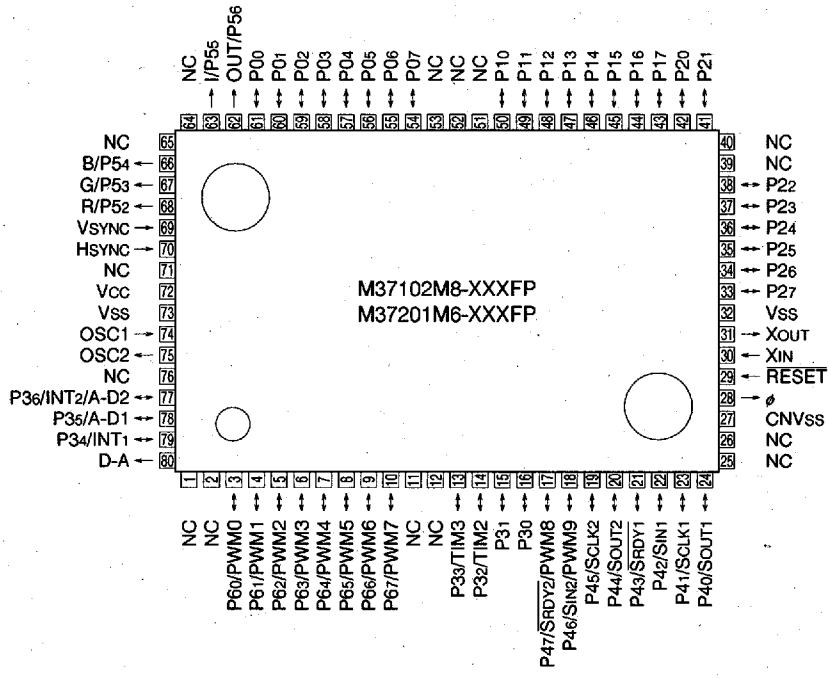
APPLICATION

TV

M37102M8-XXXSP/FP, M37102E8-XXXSP/FP, M37102E8SP/FP
M37201M6-XXXSP/FP, M37201E6-XXXSP/FP, M37201E6SP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

PIN CONFIGURATION (TOP VIEW)



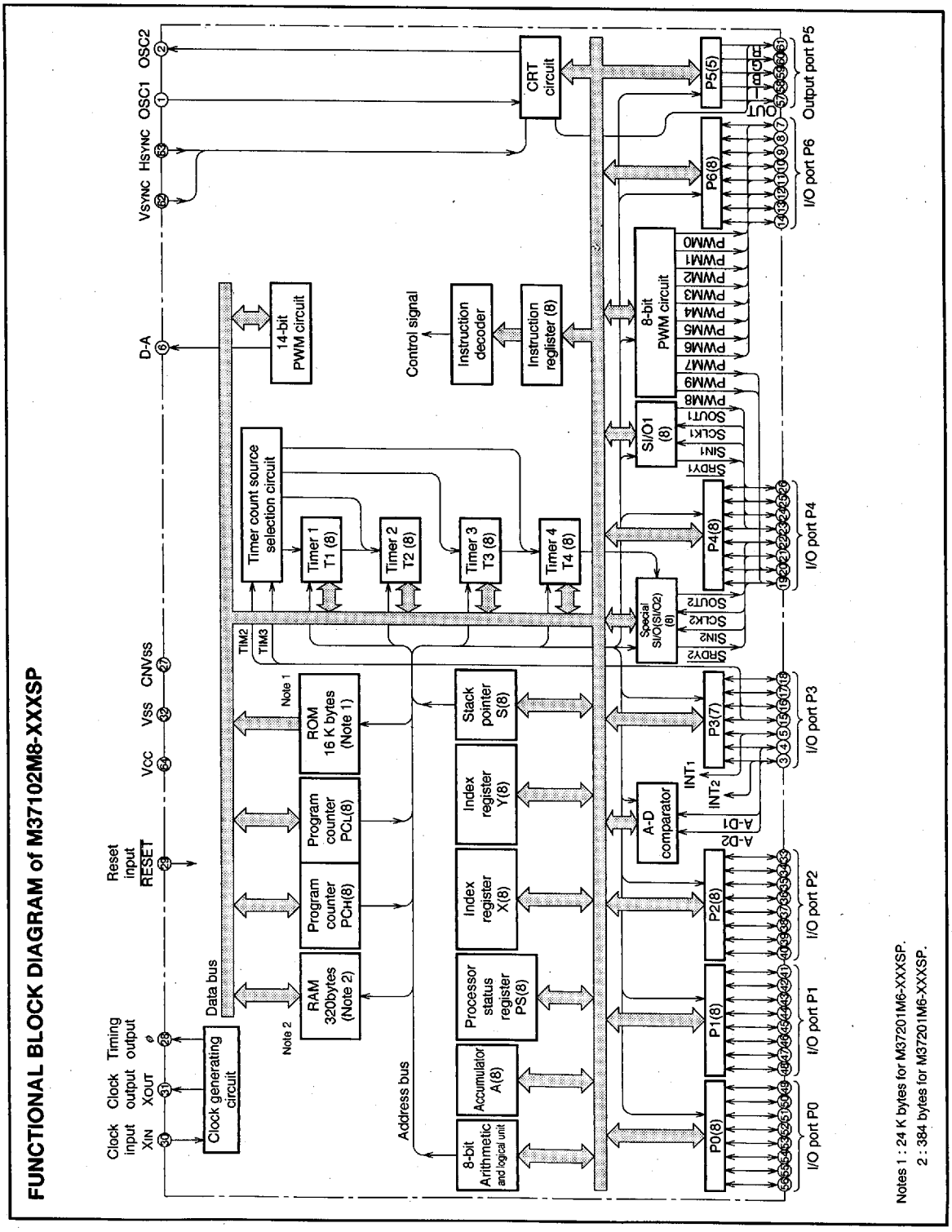
Outline 80P6N-A

NC : No connection

M37102M8-XXXSP/FP, M37102E8-XXXSP/FP, M37102E8SP/FP
M37201M6-XXXSP/FP, M37201E6-XXXSP/FP, M37201E6SP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

FUNCTIONAL BLOCK DIAGRAM of M37102M8-XXXSP



Notes 1 : 24 K bytes for M37201M6-XXXSP.
2 : 384 bytes for M37201M6-XXXSP.

MITSUBISHI ELECTRIC

M37102M8-XXXSP/FP, M37102E8-XXXSP/FP, M37102E8SP/FP
M37201M6-XXXSP/FP, M37201E6-XXXSP/FP, M37201E6SP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

FUNCTIONS

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1 μs (The minimum instruction execution time, at 4MHz oscillation frequency)
Clock frequency			4MHz
Memory size	M37102M8-XXXSP/FP	ROM	16 K bytes
		RAM	320 bytes
	M37201M6-XXXSP	ROM	24 K bytes
		RAM	384 bytes
Input/Output ports	P0, P1, P2	I/O	8-bit × 3
	$P3_0$, $P3_1$	I/O	2-bit × 1
	$P3_2$-$P3_6$	I/O	5-bit × 1 (can be used as timer input pins, INT_1, INT_2 input pins and A-D input pins)
	P4	I/O	8-bit × 1 (can be used as serial I/O function pins and PWM output pins)
	P5	Output	5-bit × 1 (can be used as R, G, B, I, OUT pins)
	P6	I/O	8-bit × 1 (can be used as PWM output pins)
Serial I/O			8-bit × 2 (Special serial I/O (8-bit) × 1)
Timers			8-bit timer × 4
Subroutine nesting			96 levels (max.)
Interrupt			Two external interrupts, nine internal interrupts, one software interrupt
Clock generating circuit			Two built-in circuits (externally connected a ceramic resonator or a quartz-crystal oscillator)
Power source voltage			5V±10%
Power dissipation	at CRT display ON		110mW (at 4MHz oscillation frequency, V_{CC} = 5.5V, Typ.)
	at CRT display OFF		55mW (at 4MHz oscillation frequency, V_{CC} = 5.5V, Typ.)
	at stop mode		1.65mW (Max.)
Operating temperature range			−10 to 70°C
Device structure			CMOS silicon gate process
Package	M37102M8-XXXSP, M37201M6-XXXSP		64-pin shrink plastic molded DIP
	M37102M8-XXXFP		80-pin plastic molded QFP
CRT display function	Number of character		24 characters × 3 lines : maximum 16 lines (by software)
	Character dot construction		12 ×16 dots
	Kinds of character		126 kinds
	Character size		4 kinds
	Kinds of color		15 kinds max. (R, G, B, I) : can be specified by character unit
	Display position (horizontal, vertical)		64 levels (horizontal) × 128 levels (vertical)

M37102M8-XXXSP/FP, M37102E8-XXXSP/FP, M37102E8SP/FP
M37201M6-XXXSP/FP, M37201E6-XXXSP/FP, M37201E6SP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Power source		Apply voltage of 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for 2μs or more (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic resonator or a quartz-crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ø	Timing output	Output	This is the timing output pin.
$P0_0$-$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
$P1_0$-$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$-$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$-$P3_6$	I/O port P3	I/O	Port P3 is a 7-bit I/O port and has basically the same functions as port P0, but the output structure of $P3_0$, $P3_1$, is CMOS output and the output structure of $P3_2$-$P3_6$, is N-channel open drain. $P3_2$, $P3_3$ are in common with external clock input pins of timer 2 and 3. $P3_4$, $P3_6$ are in common with external interrupt input pins INT_1 and INT_2. $P3_5$, $P3_6$ are in common with analog input pins of A-D comparator (A-D1, A-D2).
$P4_0$-$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain. When serial I/O1 is used, $P4_0$, $P4_1$, $P4_2$ and $P4_3$ work as S_{OUT1}, S_{CLK1}, S_{IN1} and $\overline{S_{RDY1}}$ pins, respectively. When serial I/O2 is used, $P4_4$, $P4_5$, $P4_6$ and $P4_7$ work as S_{OUT2}, S_{CLK2}, S_{IN2} and $\overline{S_{RDY2}}$ pins, respectively. Also $P4_6$, $P4_7$ are in common with PWM output pins of PWM 8 and 9.
$P6_0$-$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain. This port is in common with PWM output pins PWM0-PWM7.
OSC1, OSC2	Clock input for CRT display Clock output for CRT display	Input Output	This is the I/O pins of the clock generating circuit for the CRT display function.
H_{SYNC}	H_{SYNC} input	Input	This is the horizontal synchronizing signal input for CRT display.
V_{SYNC}	V_{SYNC} input	Input	This is the vertical synchronizing signal input for CRT display.
R, G, B, I, OUT	CRT output	Output	This is a 5-bit output pin for CRT display. The output structure is CMOS output. This is in common with port $P5_2$-$P5_6$.
D-A	DA Output	Output	This is an output pin for 14-bit PWM.

FUNCTIONAL DESCRIPTION

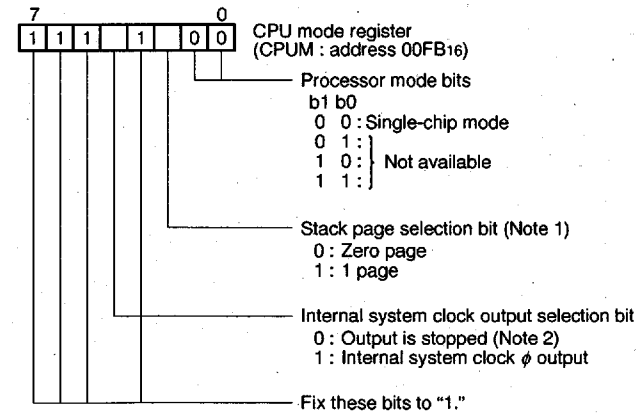
Central Processing Unit (CPU)

The M37102M8-XXXSP/FP uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:
The FST, SLW, and STP instruction cannot be used.
The WIT, MUL, and DIV instruction cannot be used.

CPU Mode Register

The CPU mode register is allocated at address $00FB_{16}$. The CPU mode register contains the stack page selection bit and the internal system clock output selection bit.



Notes 1 : Please beware of this bit when programming because it is set to "1" after the reset release.
2 : The internal system clock ϕ stoppes at "H."

Fig. 1 Structure of CPU mode register

M37102M8-XXXSP/FP, M37102E8-XXXSP/FP, M37102E8SP/FP
M37201M6-XXXSP/FP, M37201E6-XXXSP/FP, M37201E6SP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

MEMORY

Special Function Register (SFR) Area

The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for a stack area of subroutine calls and interrupts.

ROM

ROM is used for storing user programs as well as the interrupt vector area.

RAM for Display

RAM for display is used for specifing the character codes and colors to display.

ROM for Display

ROM for display is used for storing character data.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

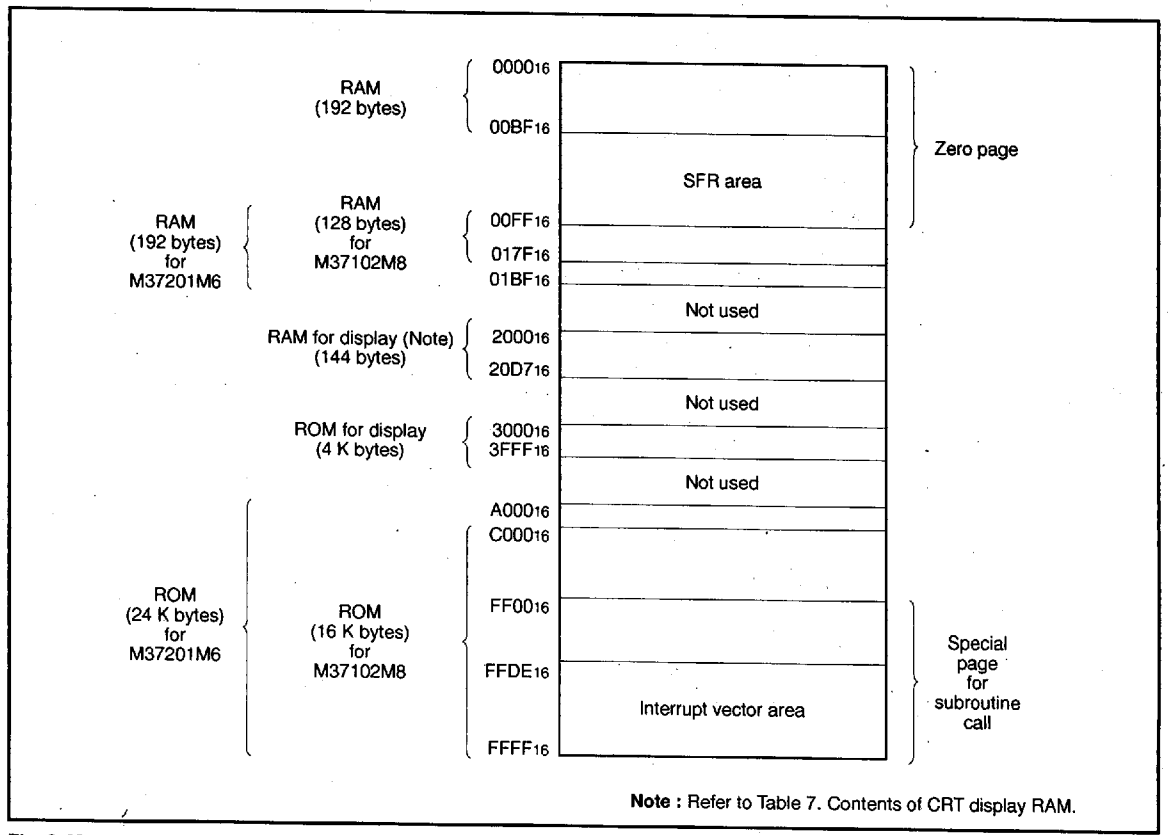
Zero Page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.



Note : Refer to Table 7. Contents of CRT display RAM.

Fig. 2 Memory map

00C0₁₆	Port P0
00C1₁₆	Port P0 directional register
00C2₁₆	Port P1
00C3₁₆	Port P1 directional register
00C4₁₆	Port P2
00C5₁₆	Port P2 directional register
00C6₁₆	Port P3
00C7₁₆	Port P3 directional register
00C8₁₆	Port P4
00C9₁₆	Port P4 directional register
00CA₁₆	Port P5
00CB₁₆	Port P5 control register
00CC₁₆	Port P6
00CD₁₆	Port P6 directional register
00CE₁₆	DA-H register
00CF₁₆	DA-L register
00D0₁₆	PWM 0 register
00D1₁₆	PWM 1 register
00D2₁₆	PWM 2 register
00D3₁₆	PWM 3 register
00D4₁₆	PWM 4 register
00D5₁₆	PWM output control register 1
00D6₁₆	PWM output control register 2
00D7₁₆	Interrupt interval determination register
00D8₁₆	Interrupt interval determination control register
00D9₁₆	Special serial I/O register
00DA₁₆	Special mode register 1
00DB₁₆	Special mode register 2
00DC₁₆	Serial I/O1 mode register
00DD₁₆	Serial I/O1 register
00DE₁₆	Serial I/O2 mode register
00DF₁₆	Serial I/O2 register

00E0₁₆	Horizontal position register
00E1₁₆	Vertical display start position register 1
00E2₁₆	Vertical display start position register 2
00E3₁₆	Vertical display start position register 3
00E4₁₆	Character size register
00E5₁₆	Border selection register
00E6₁₆	Color register 0
00E7₁₆	Color register 1
00E8₁₆	Color register 2
00E9₁₆	Color register 3
00EA₁₆	CRT control register
00EB₁₆	Display block counter
00EC₁₆	CRT port control register
00ED₁₆	Wipe control register
00EE₁₆	Wipe start register
00EF₁₆	A-D control register
00F0₁₆	Timer 1
00F1₁₆	Timer 2
00F2₁₆	Timer 3
00F3₁₆	Timer 4
00F4₁₆	Timer 12 mode register
00F5₁₆	Timer 34 mode register
00F6₁₆	PWM5
00F7₁₆	PWM6
00F8₁₆	PWM7
00F9₁₆	PWM8
00FA₁₆	PWM9
00FB₁₆	CPU mode register
00FC₁₆	Interrupt request register 1
00FD₁₆	Interrupt request register 2
00FE₁₆	Interrupt control register 1
00FF₁₆	Interrupt control register 2

Fig. 3 Memory map of special function register (SFR)

INTERRUPTS

Interrupts can be caused by 12 different sources consisting of 3 external, 8 internal, 1 software, and reset.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request bit is cleared automatically. The reset can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 4 shows the structure of the interrupt request registers 1 and 2 and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0". The interrupt request bit can be cleared with a program, but not set. The interrupt enable bit can be set and cleared with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Table 1. Interrupt vector address and priority

Interrupt source	Priority	Vector addresses	Remarks
Reset	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
CRT interrupt	2	$FFFD_{16}$, $FFFC_{16}$	
INT_2 interrupt	3	$FFFB_{16}$, $FFFA_{16}$	Active edge selectable
INT_1 interrupt	4	$FFF9_{16}$, $FFF8_{16}$	Active edge selectable
Serial I/O2 interrupt	5	$FFF7_{16}$, $FFF6_{16}$	
Timer 4 interrupt	6	$FFF5_{16}$, $FFF4_{16}$	
1 ms interrupt (Note)	7	$FFF3_{16}$, $FFF2_{16}$	
V_{SYNC} interrupt	8	$FFF1_{16}$, $FFF0_{16}$	Active edge selectable
Timer 3 interrupt	9	$FFEF_{16}$, $FFEE_{16}$	
Timer 2 interrupt	10	$FFED_{16}$, $FFEC_{16}$	
Timer 1 interrupt	11	$FFEB_{16}$, $FFEA_{16}$	
Serial I/O1 interrupt	12	$FFE9_{16}$, $FFE8_{16}$	
BRK instruction interrupt	13	$FFDF_{16}$, $FFDE_{16}$	Non-maskable software interrupt

Note : At $f(X_{IN})$ = 4 MHz.

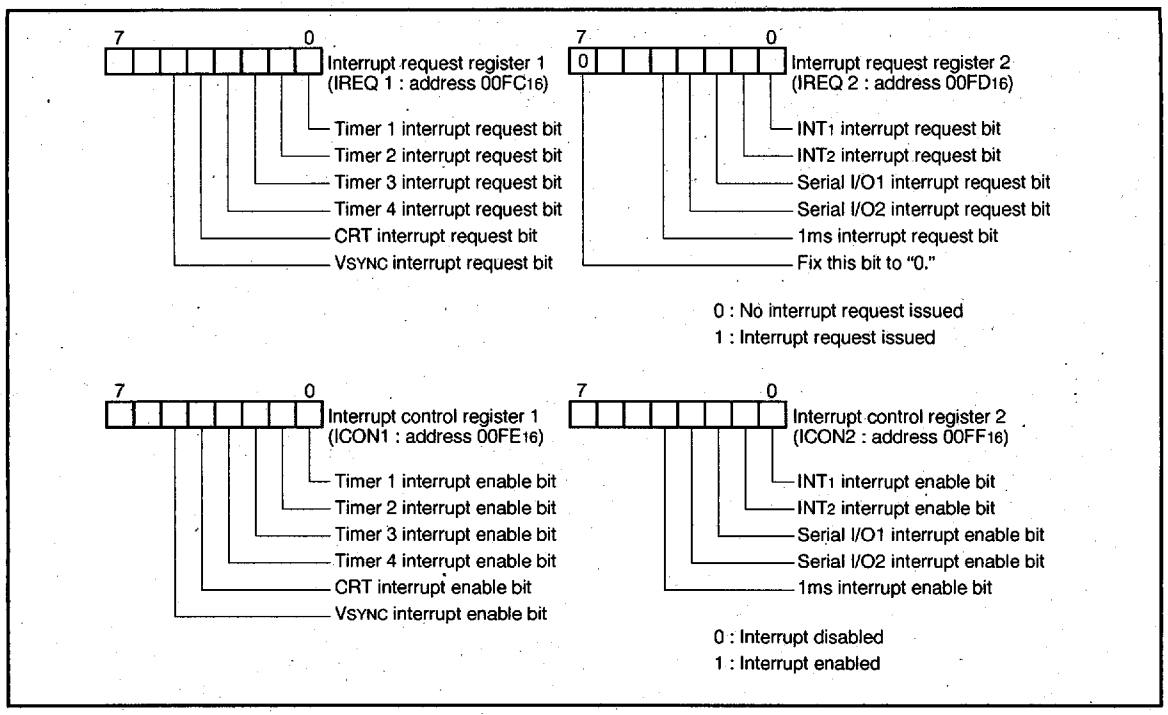


Fig. 4 Structure of interrupt-related registers

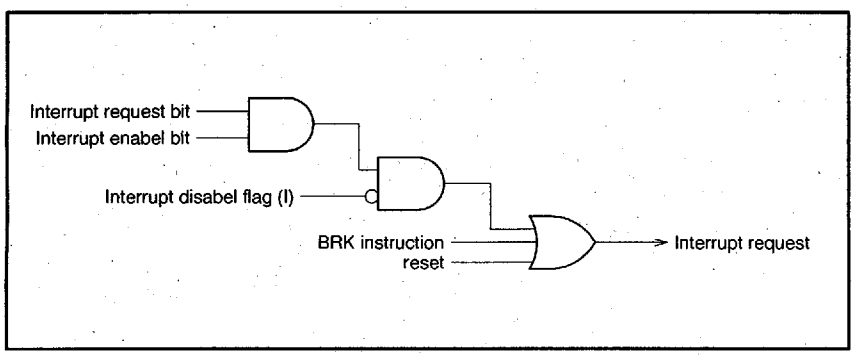


Fig. 5 Interrupt control

TIMERS

The M37102M8-XXXSP/FP has 4 timers: timer 1, timer 2, timer 3, and timer 4. All timers are 8-bit timers with the 8-bit timer latch. The timer block diagram is shown in Figure 7.

All of the timers count down and their divide ratio is 1/(n+1), where n is the value of timer latch. The value is set to a timer at the same time by writing a count value to the corresponding timer latch (addresses $00F0_{16}$ to $00F3_{16}$: timers 1 to 4).

The count value is decremented by 1. The timer interrupt request bit is set to "1" by an timer overflow at the next count pulse after the count value reaches "00_{16}."

(1) Timer 1

Timer 1 can select one of the following count sources:

- f(XIN)/16
- f(XIN)/4096 (1 ms interrupt signal)

The count source of timer 1 is selected by setting bit 0 of the timer 12 mode register (address $00F4_{16}$).

Timer 1 interrupt request occurs at timer 1 overflow.

(2) Timer 2

Timer 2 can select one of the following count sources:

- f(XIN)/16
- Timer 1 overflow signal
- External clock from the P32/TIM2 pin

The count source of timer 2 is selected by setting bits 4 and 1 of the timer 12 mode register (address $00F4_{16}$). When timer 1 overflow signal is a count source for the timer 2, the timer 1 functions as an 8-bit prescaler.

Timer 2 interrupt request occurs at timer 2 overflow.

(3) Timer 3

Timer 3 can select one of the following count sources:

- f(XIN)/16
- External clock from the P33/TIM3 pin

The count source of timer 3 is selected by setting bit 0 of the timer 34 mode register (address $00F5_{16}$).

Timer 3 interrupt request occurs at timer 3 overflow.

(4) Timer 4

Timer 4 can select one of the following count sources:

- f(XIN)/16
- f(XIN)/2
- Timer 3 overflow signal

The count source of timer 3 is selected by setting bits 4 and 1 of the timer 34 mode register (address $00F5_{16}$). When timer 3 overflow signal is a count source for the timer 4, the timer 3 functions as an 8-bit prescaler.

Timer 4 interrupt request occurs at timer 4 overflow. And besides, the timer 4 overflow signal is also used as the clock source of special serial I/O.

At reset, timers 3 and 4 are connected by hardware and "FF_{16}" is automatically set in timer 3; "07_{16}" in timer 4. The f(XIN)/16 is selected as the timer 3 count source. The internal reset is released by timer 4 overflow at these state, the internal clock is connected .

At execution of the STP instruction, timers 3 and 4 are connected by hardware and "FF_{16}" is automatically set in timer 3; "07_{16}" in timer 4. However, the f(XIN)/16 is not selected as the timer 3 count source. So set bit 0 of the timer 34 mode register (address $00F5_{16}$) to "0" before the execution of the STP instruction (f(XIN)/16 is selected as the timer 3 count source). The internal STP state is released by timer 4 overflow at these state, the internal clock is connected .

Because of this, the program starts with stable clock.

The structure of timer-related registers is shown in Figure 6.

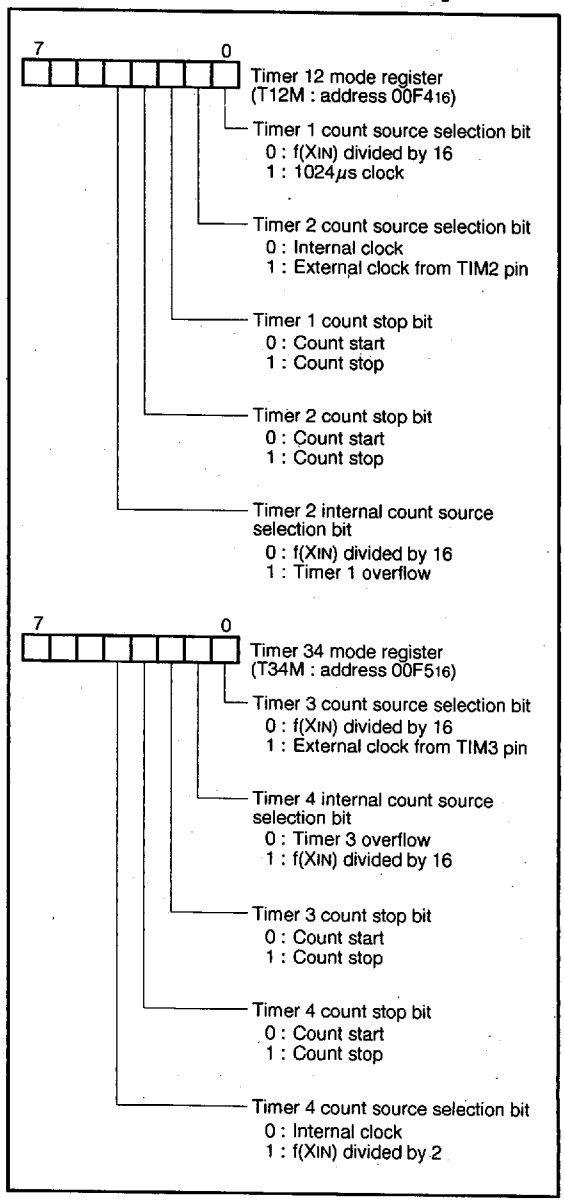
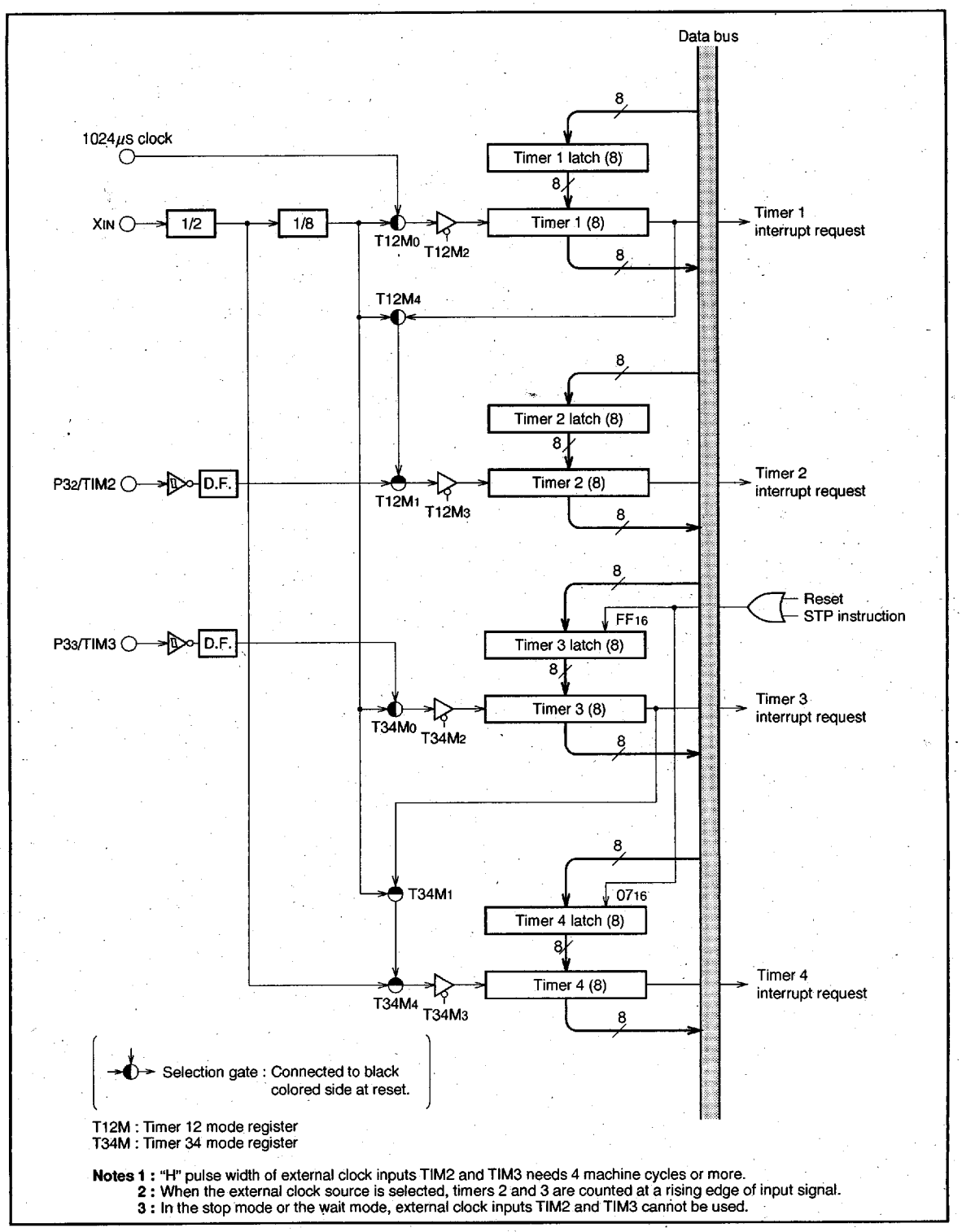


Fig. 6 Structure of timer-related registers



Notes 1 : "H" pulse width of external clock inputs TIM2 and TIM3 needs 4 machine cycles or more.
2 : When the external clock source is selected, timers 2 and 3 are counted at a rising edge of input signal.
3 : In the stop mode or the wait mode, external clock inputs TIM2 and TIM3 cannot be used.

Fig. 7 Timer block diagram

SERIAL I/O

M37102M8-XXXSP has two serial I/O (serial I/O1, serial I/O2). Serial I/O1 has the same function as serial I/O2.

A block diagram of the serial I/O is shown in Figure 8.

In the serial I/O mode the receive ready signal ($\overline{S_{RDYi}}$), synchronous input/output clock (S_{CLKi}), and the serial I/O pins (S_{OUTi}, S_{INi}) are used as port P4. The serial I/O$_i$ mode registers (address $00DC_{16}$, $00DE_{16}$) are 8-bit registers. Bits 0, 1 and 2 of these registers are used to select a synchronous clock source.

Bit 3 and 4 decide whether parts of P4 will be used as a serial I/O or not.

To use $P4_2$ or $P4_6$ as a serial input, set the directional register bit which corresponds to $P4_2$ or $P4_6$ to "0". For more information on the directional register, refer to the I/O pin section.

Also to use internal clock of serial I/O2, bit 1 of special mode register 1 (address $00DA_{16}$) needs to be set to "1".

The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

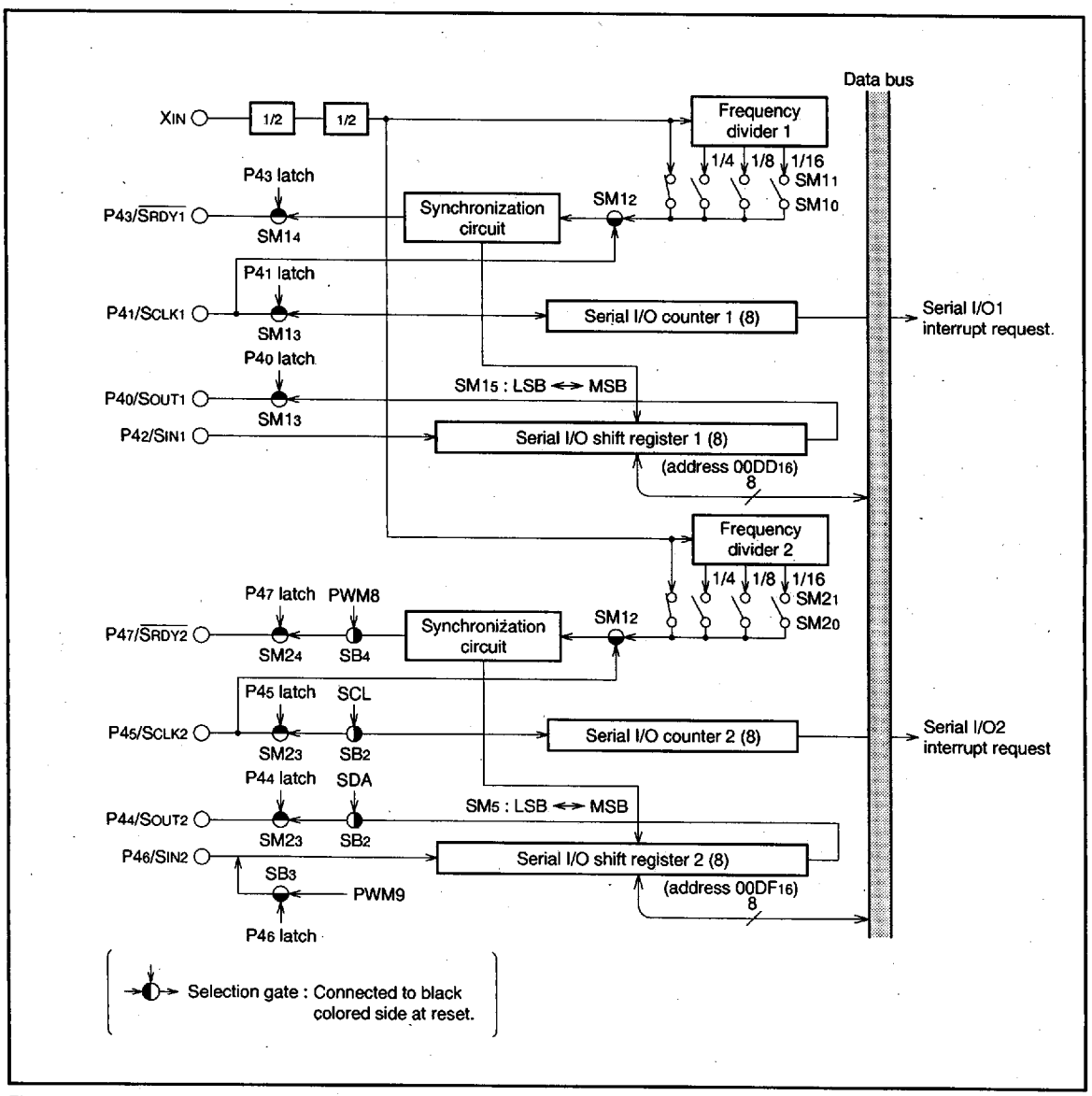


Fig. 8 Block diagram of serial I/O

Internal clock—The $\overline{SRDYi}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O$_i$ register (address $00DD_{16}$, $00DF_{16}$). After the falling edge of the write signal, the $\overline{SRDYi}$ signal becomes low signaling that the M37102M8-XXXSP is ready to receive the external serial data. The $\overline{SRDYi}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O$_i$ counter is set to 7 when data is stored in the serial I/O$_i$ register. At each falling edge of the transfer clock, serial data is output to S_{OUTi}. During the rising edge of this clock, data can be input from S_{INi} and the data in the serial I/O$_i$ register will be shifted 1 bit.

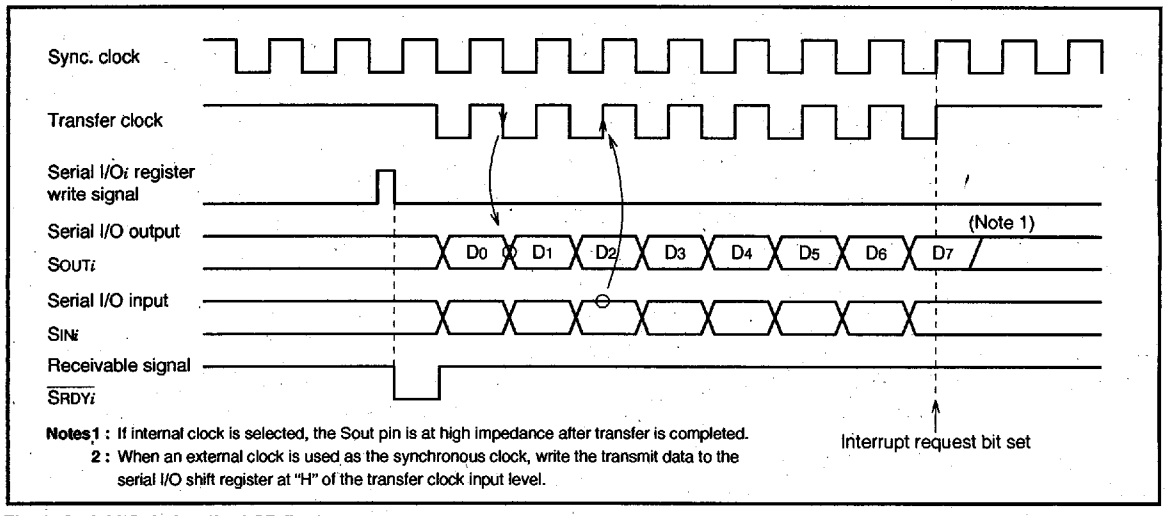
Transfer direction can be selected by bit 5 of serial I/O$_i$ mode register. After the transfer clock has counted 8 times, the serial I/O$_i$ register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External clock— If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 500kHz at a duty cycle of 50%. The timing diagram is shown in Figure 9. When using an external clock for transfer, the external clock must be held at "H" level when the serial I/O$_i$ counter is initialized. When switching between the internal clock and external clock, the switching must not be performed during transfer. Also, the serial I/O counter must be initialized after switching.

An example of communication between two M37102M8-XXXSPs is shown in Figure 10.

Notes 1 : On programming, note that the serial I/O counter is set by writing to the serial I/O register with the bit managing instructions as SEB and CLB instructions.
2 : When an external clock is used as the synchronizing clock, write transmit data to the serial I/O register at "H" of the transfer clock input level.



Notes 1 : If internal clock is selected, the Sout pin is at high impedance after transfer is completed.
2 : When an external clock is used as the synchronous clock, write the transmit data to the serial I/O shift register at "H" of the transfer clock input level.

Fig. 9 Serial I/O timing (for LSB first)

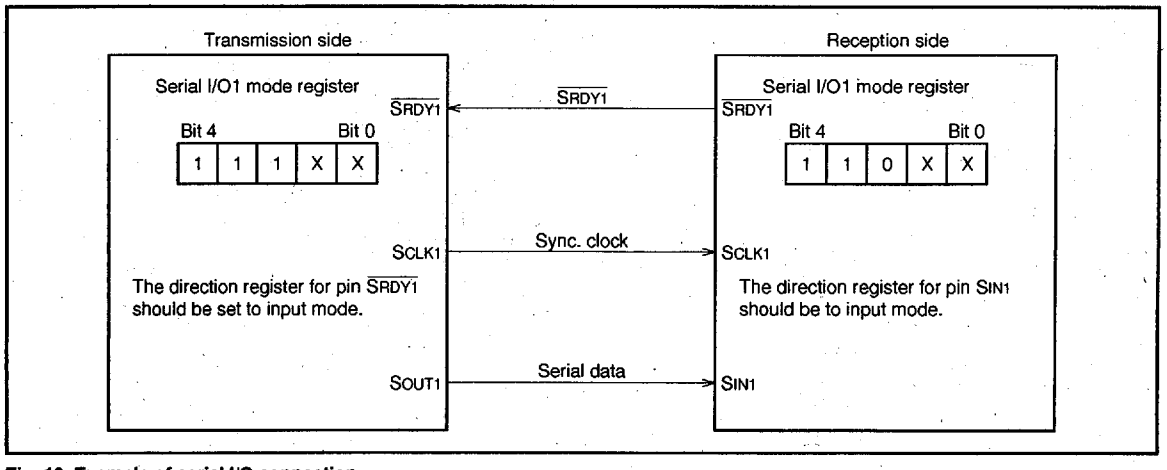


Fig. 10 Example of serial I/O connection

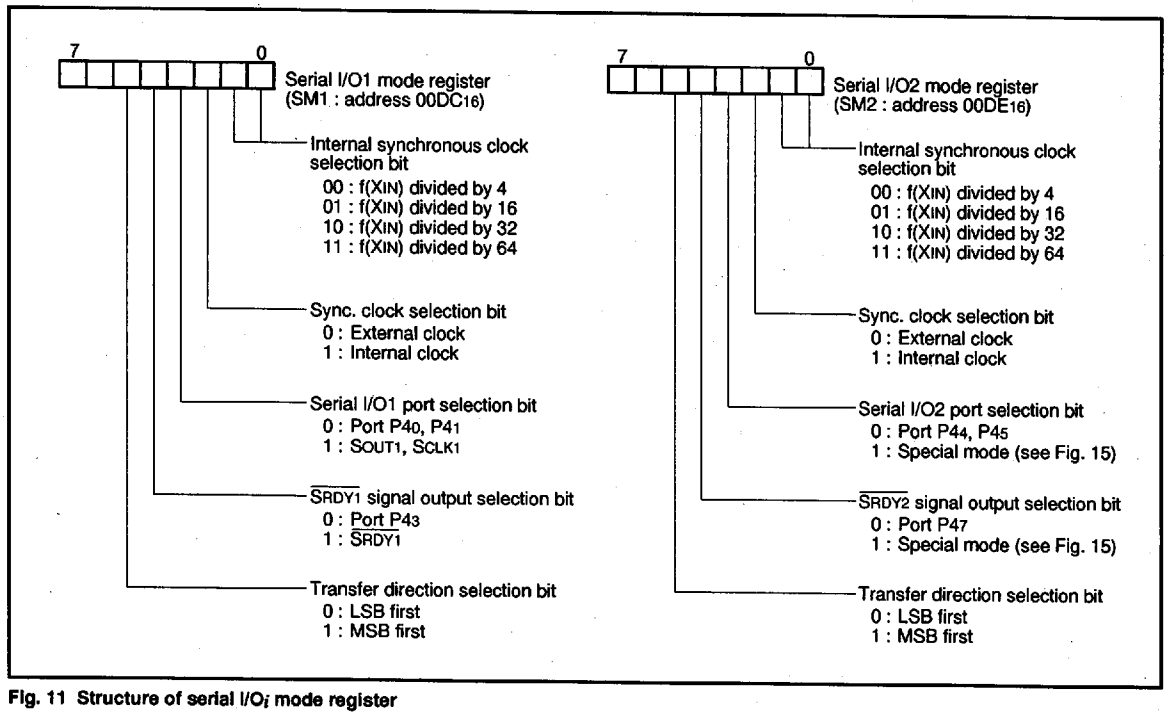


Fig. 11 Structure of serial I/O$_i$ mode register

SPECIAL MODE (I^2C BUS MODE*)

M37102M8-XXXSP has a special serial I/O circuit that can be reception or transmission of serial data in conformity with I^2C (Inter IC) bus format.

I^2C bus is a two line directional serial bus developed by Philips to transfer and control data between one IC and the other IC in machinery.

M37102M8-XXXSP's special serial I/O is not included the clock synchronisation function and the arbitration detectable function at multimaster.

Operations of master transmission and master reception with special serial I/O are explained in the following:

(1) Master Transmission

To generate an interrupt at the end of transmission, set bit 7 of special mode register 2 (address $00DB_{16}$) to "1" so as to special mode serial I/O interrupt is selected. Then set bit 3 of interrupt control register 2 (address $00FF_{16}$) to "1" so as to special mode serial I/O interrupt is enabled. Clear the interrupt disable flag I to "0" by using the CLI instruction.

The output signals of master transmission SDA and SCL are output from ports $P4_4$ and $P4_5$. Set all bits (bits 4 and 5) corresponding to $P4_4$ and $P4_5$ of the port P4 register (address $00C8_{16}$) and the port P4 direction register (address $00C9_{16}$) to "1".

Set the transmission clock. The transmission clock uses the overflow signal of timer 4. Set appropriate value in timer 4. (For instance, if $f(X_{IN})/16$ is selected as the clock source of timer 4 and 4 is set in timer 4 when $f(X_{IN})$ is 4MHz, the master transmission clock frequency is 25kHz.)

Set contents of the special mode register 2 (address $00DB_{16}$). (Usually, "83_{16}".)

Set the bit 3 of serial I/O2 mode register (address $00DE_{16}$).

After that set the special mode register 1 (address $00DA_{16}$). Figure 15 shows the structure of special mode registers 1 and 2.

Initial setting is completed by the above procedure.

Write data to be transmitted in the special serial I/O register (address $00D9_{16}$). Immediately after this, clear bits 0 and 1 of special mode register 2 (to "0") to make both SDA and SCL output to "L". This is for arbitration. The start signal has been completed.

The hardware automatically sends out data of 9-clock cycle. The 9th clock is for ACK reception and the output level becomes "H" at this clock. If other master outputs the start signal to transmit data simultaneously with this 9th clock, it is not detected as an arbitration-lost.

When the ACK bit has been transmitted, bit 3 of the interrupt request register 2 is set to "1" (issue of interrupt request), notifying the end of data transmission.

To transmit data successively, write data to be sent to the special serial I/O register, and set the interrupt enabled state again. By repeating this procedure, unlimited number of bytes can be transmitted.

To terminate data transfer, clear bits 0 and 1 of the special mode register to "0", set bit 1 clock SCL to "1", then set bit 1 data SDA to "1". This procedure transmits the stop signal.

Figure 13 shows master transmission timing explained above.

(2) Master Reception

Master reception is carried out in the interrupt routine after data is transferred by master transmission. For master transmission and interrupt thereafter, see the preceding section (1) Master transmission.

In the interrupt routine, set master reception ACK provided (26_{16}) in the special mode register 1 (address $00DA_{16}$), and write "FF_{16}" in the special serial I/O register (address $00D9_{16}$). This sets data line SDA to "H" and to perform 8-clock master reception. Then, "L" is transmitted to data line SDA for ACK receiving. In the ACK provided mode, the above ACK is automatically sent out.

Repeat the above receiving operation for a necessary number of times. Then return to the master transmission mode and transmit the stop signal by the same procedure for the master transmission.

Figure 14 shows master reception timing.

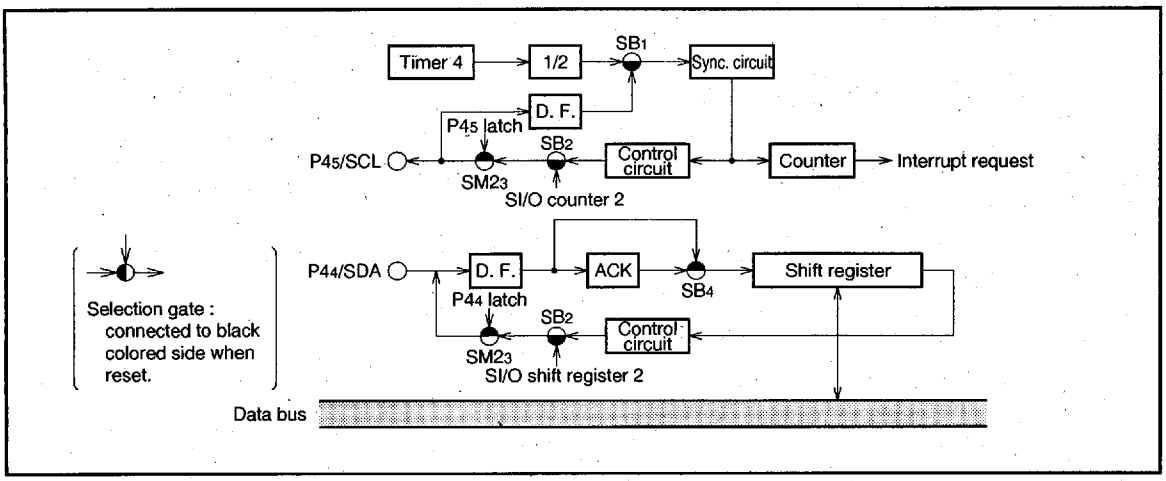


Fig. 12 Block diagram of special serial I/O

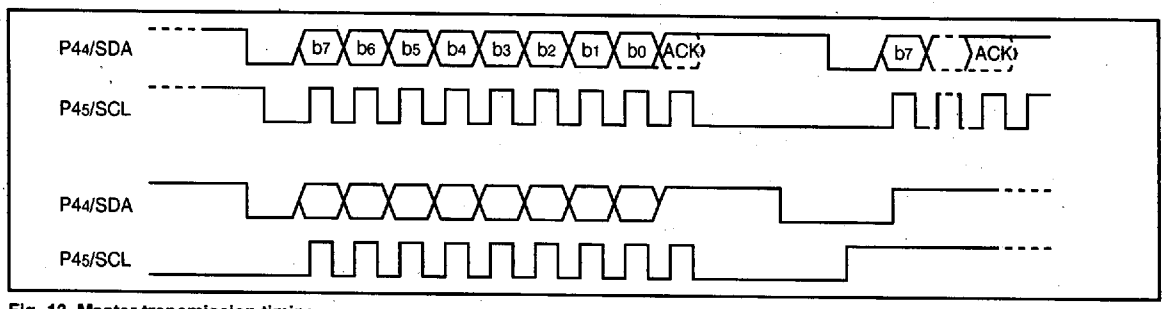


Fig. 13 Master transmission timing

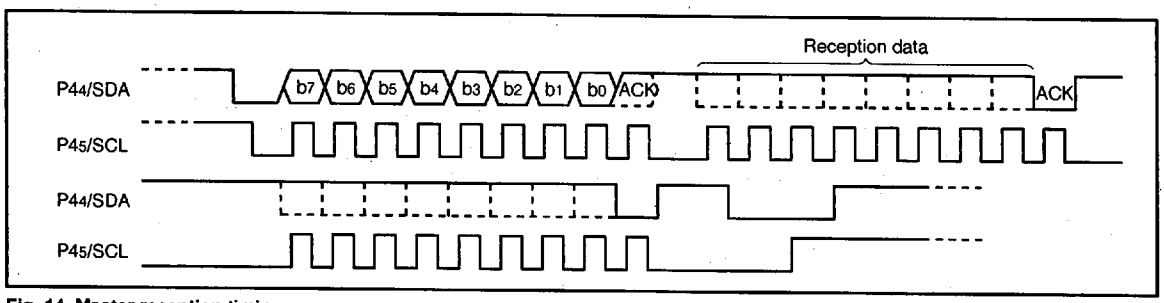


Fig. 14 Master reception timing

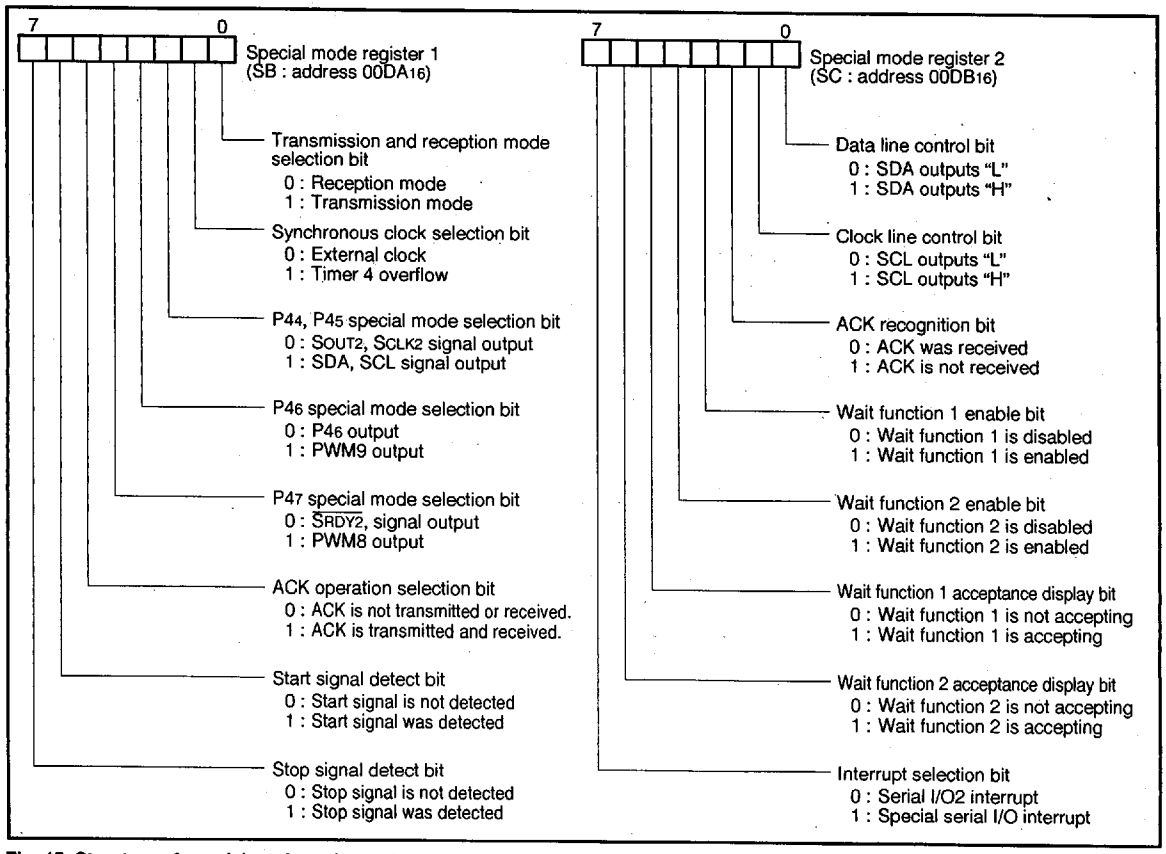


Fig. 15 Structure of special mode registers 1 and 2

PWM OUTPUT CIRCUIT

(1) Introduction

The M37102M8-XXXSP is equipped with one 14-bit PWM (DA) and ten 8-bit PWMs (PWM0-PWM9). The 14-bit resolution gives DA the minimum resolution bit width of 500ns (for f(X_{IN})=4MHz) and a repeat period of 8192μs. PWM0-PWM9 have a 8-bit resolution with minimum resolution bit width of 8μs and repeat period of 2048μs.

Block diagram of the PWM is shown in Figure 16.

The PWM timing generator section applies individual control signals to DA and PWM0-9 using clock input X_{IN} divided by 2 as a reference signal.

(2) Data Setting

The output pins PWM0-7 are in common with port P6 and PWM8, 9 are in common with port $P4_6$, $P4_7$.

For PWM output, each PWM output selection bit (bit 1 to 7 of PWM output control register 1, bit 0, 1 of PWM output control register 2, bit 3, 4 of special mode register 1 and bit 4 of serial I/O2 mode register) should be set. When DA is used for output, first set the higher 8-bit of the DA-H register (address $00CE_{16}$), then the lower 6-bit of the DA-L register (address $00CF_{16}$).

When one of the PWM0-9 is used for output, set the 8-bit in the PMM0-9 register (address $00D0_{16}$ to $00D4_{16}$, $00F6_{16}$ to $00FA_{16}$), respectively.

(3) Transferring Data from Registers to Latches

The data written to the PWM registers is transferred to the PWM latches at the repetition of the PWM period.

The signals output to the PWM pins correspond to the contents of these latches. When data in each PWM register is read, data in these latches has already been read allowing the data output by the PWM to be confirmed. However, bit 7 of the DA-L register indicated the completion of the data transfer from the DA register to the DA latch. If bit 7 is "0", the transfer has been completed, if bit 7 is "1", the transfer has not yet begun.

(4) Operation of the 8-bit PWMs

The timing diagram of the ten 8-bit PWMs (PWM0-9) is shown in Figure 17. One period (T) is composed of 256(2^8) segments.

There are eight different pulse types configured from bits 0 to 7 representing the significance of each bit. These are output within one period in the circuit internal section. Refer to Figure 17 (a). Eight different pulses can be output from the PWM.

These can be selected by bits 0 through 7. Depending on the content of the 8-bit PWM latch, pulses from 7 to 0 is selected. The PWM output is the difference of the sum of each of these pulses. Several examples are shown in Figure 17 (b). Changes in the contents of the PWM latch allows the selection of 256 lengths of high-level area outputs varying from 0/256 to 255/256. A length of entirely high-level output cannot be output, i.e. 256/256.

(5) 14-bit PWM Operation

The output example of the 14-bit PWM is shown in Figure 18. The 14-bit PWM divides the data within the PWM latch into the lower 6 bits and higher 8 bits.

A high-level area within a length D_H times τ is output every short area of t=256 τ=128μs as determined by data D_H of the higher 8 bits.

Thus, the time for the high-level area is equal to the time set by the lower 8 bits or that plus τ. As a result, the short-area period t (=128μs, approx. 7.8kHz) becomes an approximately repetitive period.

(6) Output after Reset

At reset the output of port P4, P6 is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, its data is transferred to the latch.

Table 2. Relation between the low-order 6 bits of data and high-level area increase space

6 low-order bits of data (LSB)	Area longer by τ than that of other t_m (m=0 to 63)
0 0 0 0 0 0	Nothing
0 0 0 0 0 1	m = 32
0 0 0 0 1 0	m = 16, 48
0 0 0 1 0 0	m = 8, 24, 40, 56
0 0 1 0 0 0	m = 4, 12, 20, 28, 36, 44, 52, 60
0 1 0 0 0 0	m = 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m = 1, 3, 5, 7, ... 57, 59, 61, 63

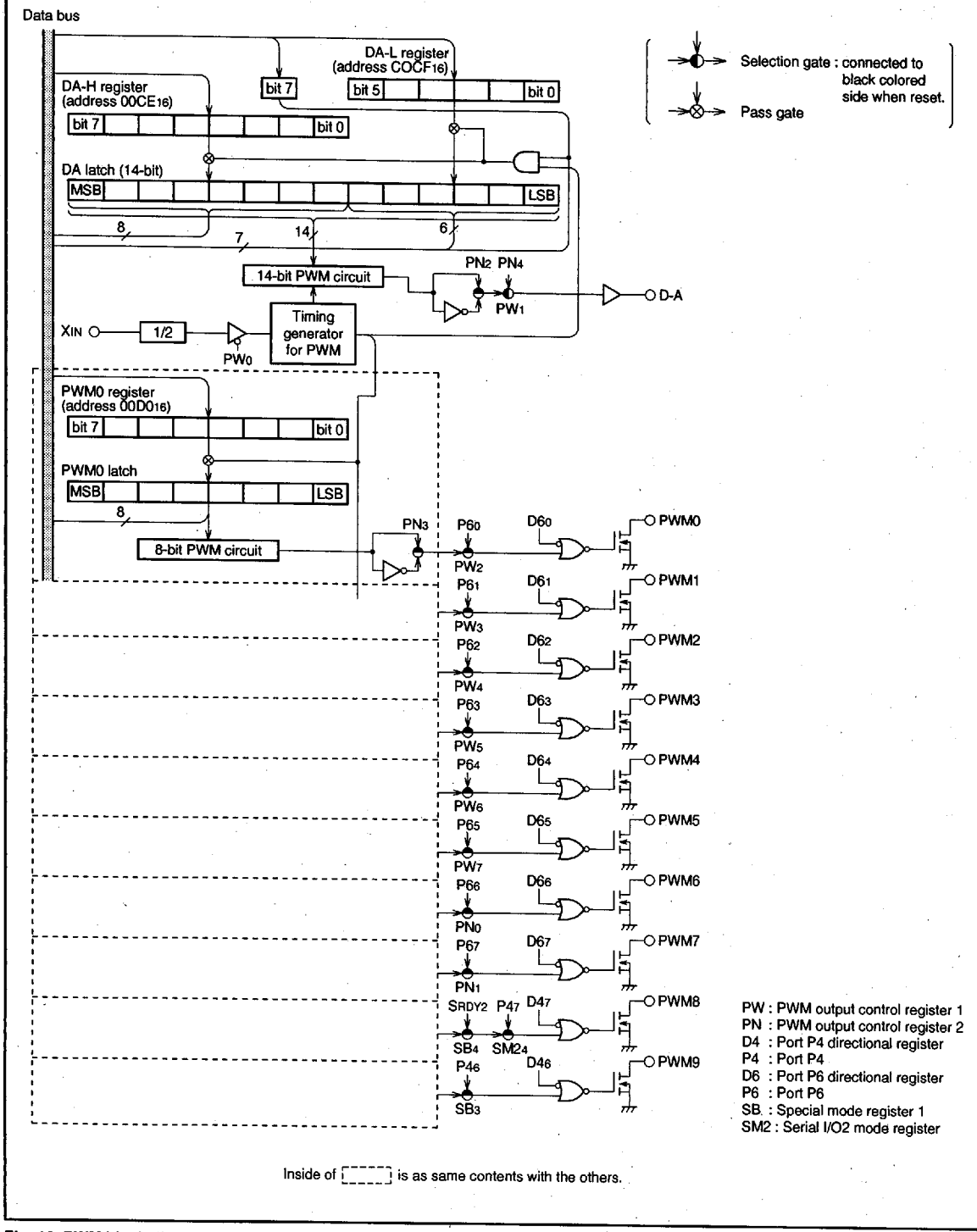


Fig. 16 PWM block diagram

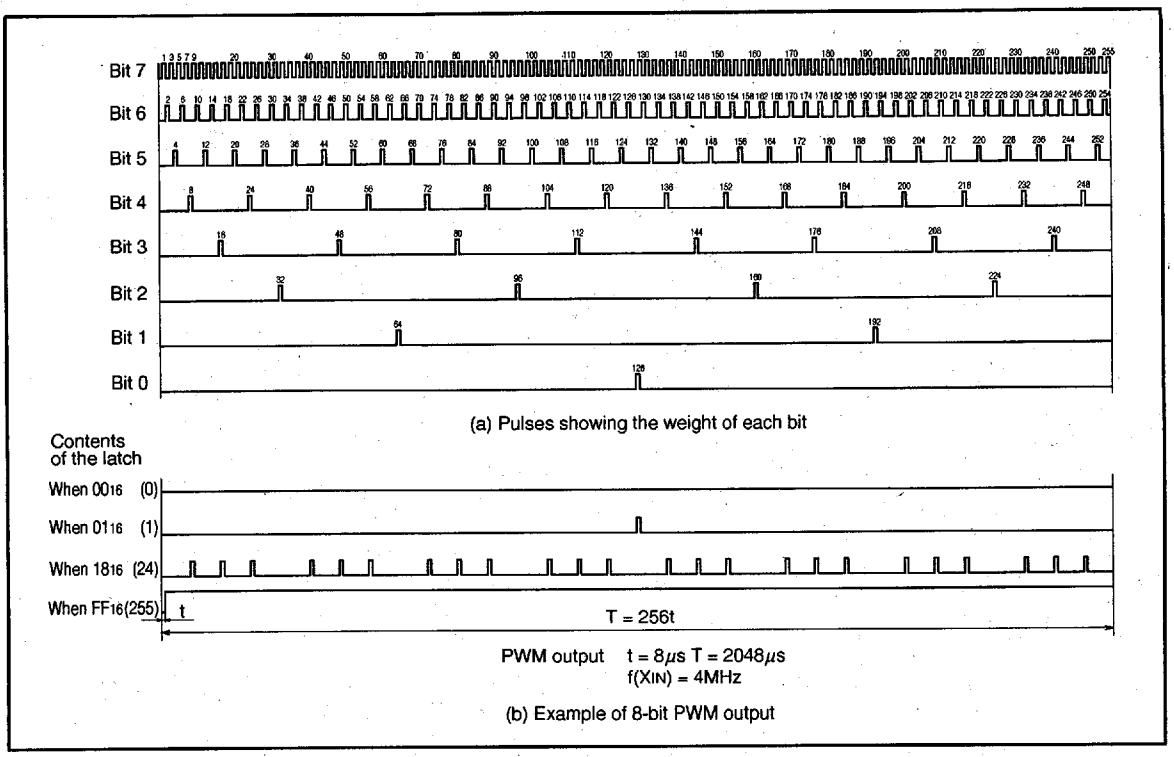


Fig. 17 8-bit PWM timing

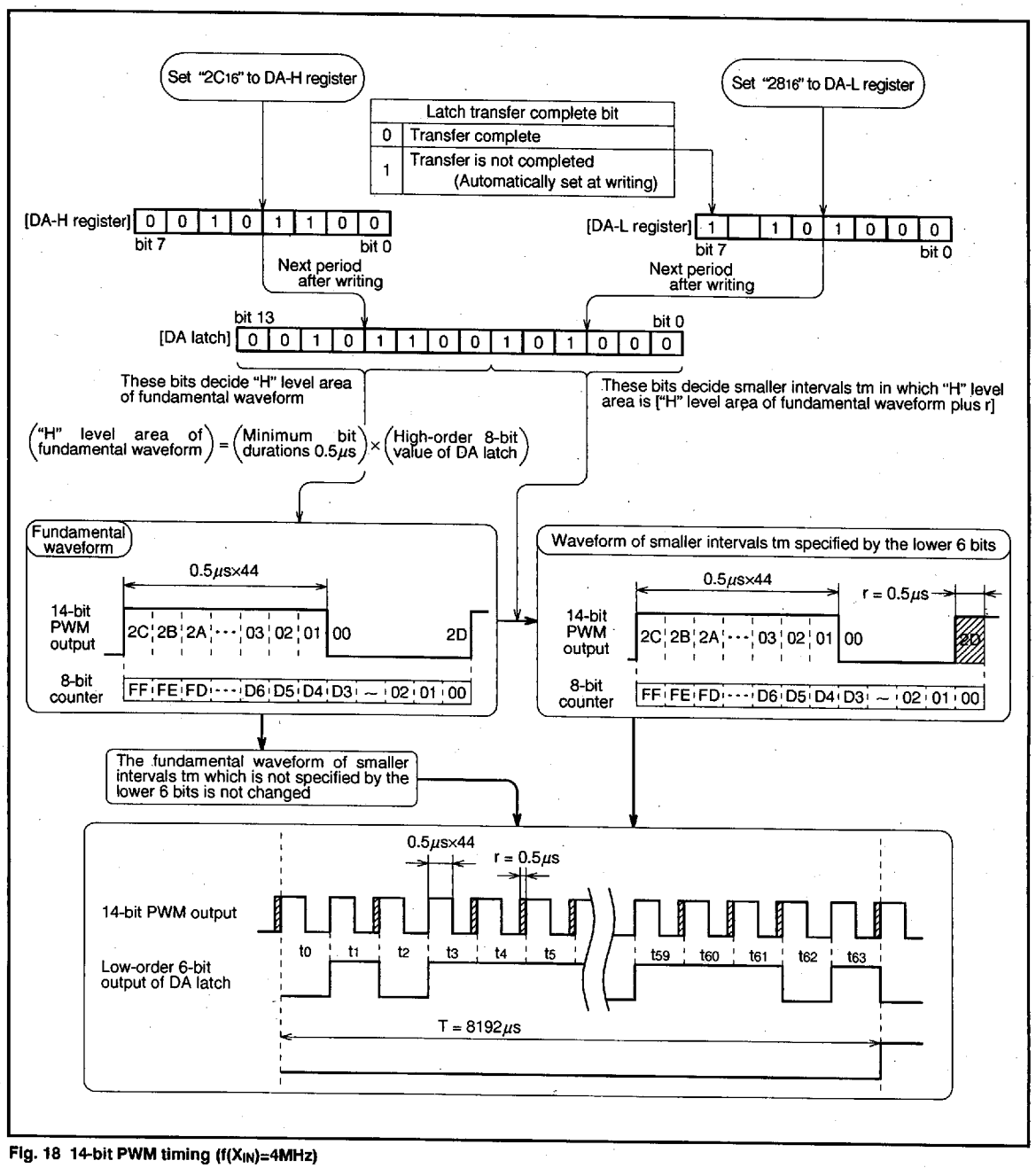


Fig. 18 14-bit PWM timing ($f(X_{IN})$=4MHz)

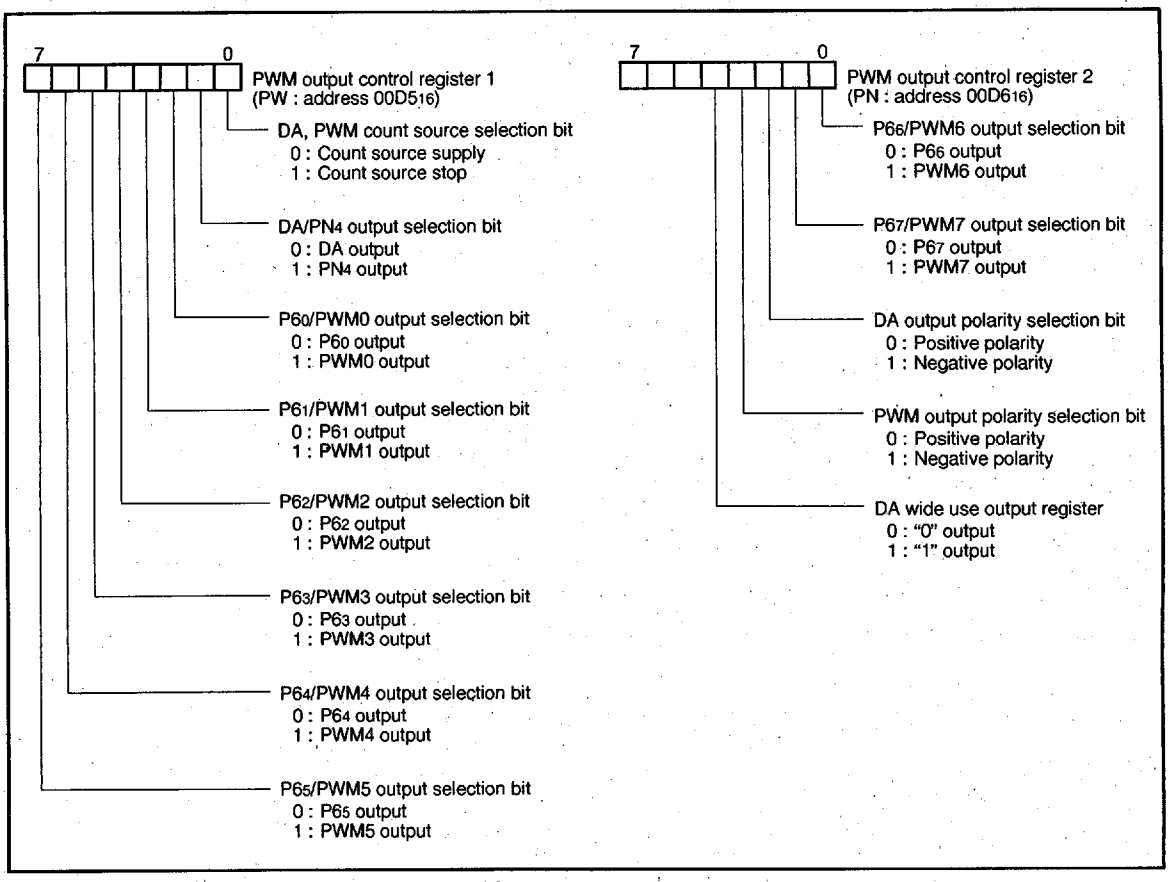


Fig. 19 Structure of PWM output control register 1 and 2

A-D COMPARATOR

Block diagram of A-D comparator is shown in Figure 21. A-D comparator consists of 4-bit D-A converter and comparator.

The A-D control register can generate 1/16 V_{CC}-step internal analog voltage based on the settings of bits 0 to 3.

Table 3 gives the relation between the descriptions of A-D control register bits 0 to 3 and the generated internal analog voltage. The comparison result of the analog input voltage and the internal analog voltage is stored in the A-D control register, bit 4.

The data is compared by setting the direction register corresponding to port $P3_5$, $P3_6$ to "0" (port $P3_5$, $P3_6$ enters the input mode), to allow port $P3_5$/A-D1, $P3_6$/A-D2 to be used as the analog input pin. The digital value corresponding to the internal analog voltage to be compared is then written in the A-D control register, bit 0 to 3 and an analog input pin is selected. After 16 machine cycle, the voltage comparison starts.

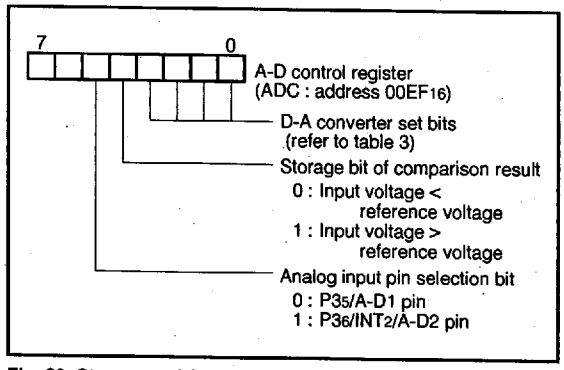


Fig. 20 Structure of A-D control register

Table 3. Relationship between the contents of A-D control register and reference voltage

A-D control register				Reference voltage
Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	1/32 V_{CC}
0	0	0	1	3/32 V_{CC}
0	0	1	0	5/32 V_{CC}
0	0	1	1	7/32 V_{CC}
0	1	0	0	9/32 V_{CC}
0	1	0	1	11/32 V_{CC}
0	1	1	0	13/32 V_{CC}
0	1	1	1	15/32 V_{CC}
1	0	0	0	17/32 V_{CC}
1	0	0	1	19/32 V_{CC}
1	0	1	0	21/32 V_{CC}
1	0	1	1	23/32 V_{CC}
1	1	0	0	25/32 V_{CC}
1	1	0	1	27/32 V_{CC}
1	1	1	0	29/32 V_{CC}
1	1	1	1	31/32 V_{CC}

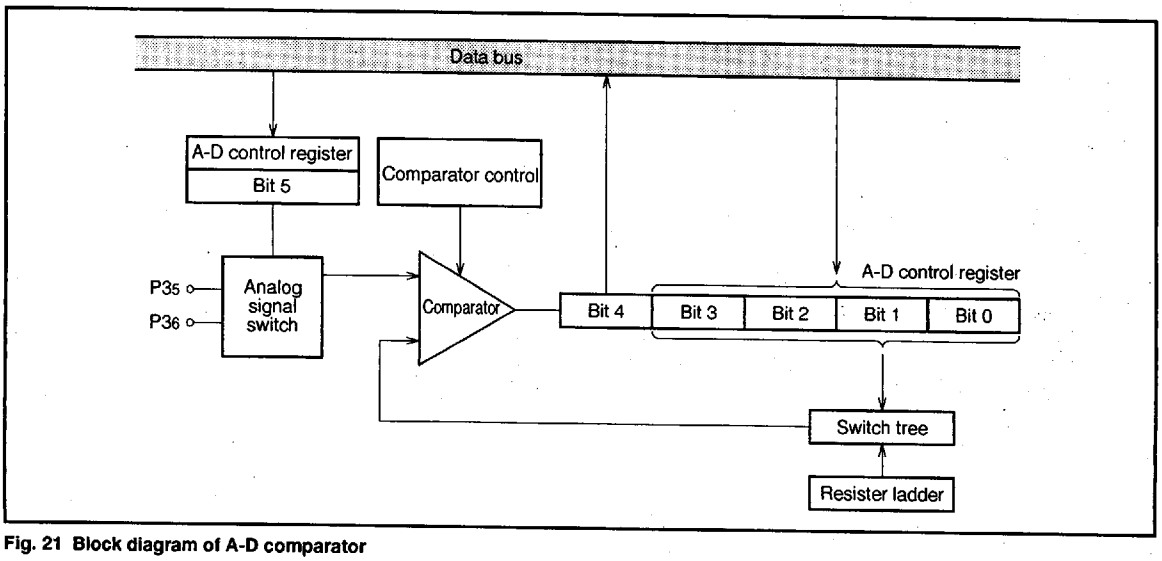


Fig. 21 Block diagram of A-D comparator

M37102M8-XXXSP/FP, M37102E8-XXXSP/FP, M37102E8SP/FP
M37201M6-XXXSP/FP, M37201E6-XXXSP/FP, M37201E6SP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

CRT DISPLAY FUNCTIONS

(1) Outline of CRT Display Functions

Table 4 outlines the CRT display functions of the M37102M8-XXXSP. The M37102M8-XXXSP incorporates a 24 columns × 3 lines CRT display control circuit. CRT display is controlled by the CRT display control register.

Up to 126 kinds of characters can be displayed, and colors can be specified for each character. Four colors can be displayed on one screen. A combination of up to 15 colors can be obtained by using each output signal (R, G, B, and I).

Characters are displayed in a 12 × 16 dot configuration to obtain smooth character patterns (refer to Figure 22).

The following shows the procedure how to display characters on the CRT screen.

Table 4. Outline of CRT display functions

Parameter		Functions
Number of display character		24 characters × 3 lines
Character configuration		12 × 16 dots (refer to Figure 22)
Kinds of character		126
Character size		4 size selectable
Color	Kinds of color	1 screen.: 4 kinds, maximum 15 kinds
	Coloring unit	A character
Display expansion		Possible (multiline display)
Raster coloring		Possible (maximum 15 kinds)

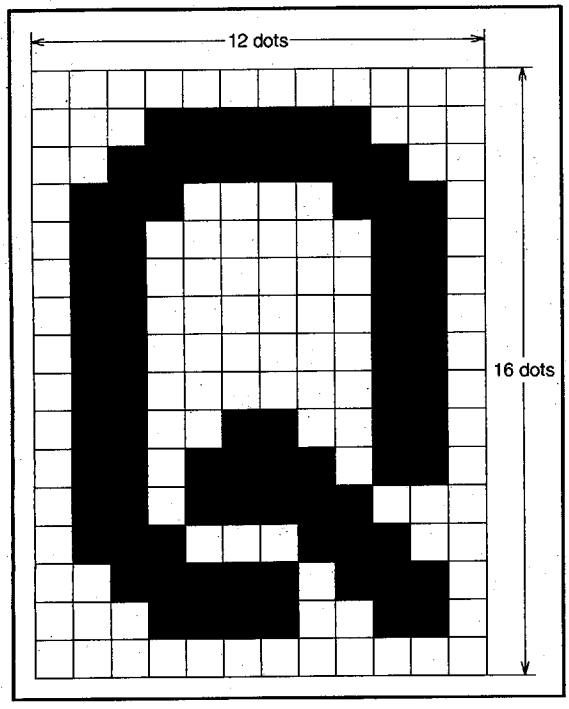


Fig. 22 CRT display character configuration

① Set the character to be displayed in display RAM.
② Set the display color by using the color register.
③ Specify the color register in which the display color is set by using the display RAM.
④ Specify the vertical position and character size by using the vertical position register and the character size register.
⑤ Specify the horizontal position by using the horizontal position register.
⑥ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT starts operation according to the input of the V_{SYNC} signal.

The CRT display circuit has an extended display mode.

This mode allows multiple lines (more than 4 lines) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 24 shows a block diagram of the CRT display control circuit. Figure 23 shows the structure of the CRT display control register.

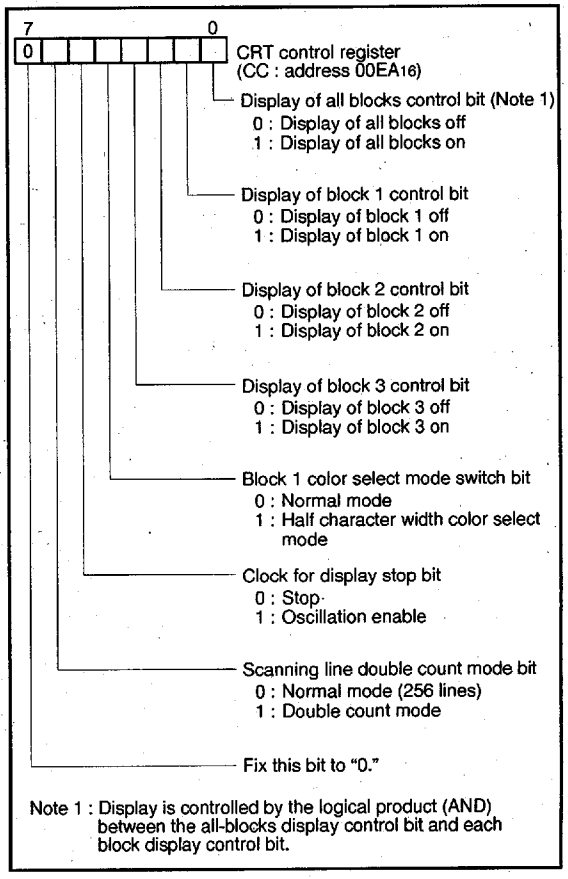


Fig. 23 Structure of CRT control register

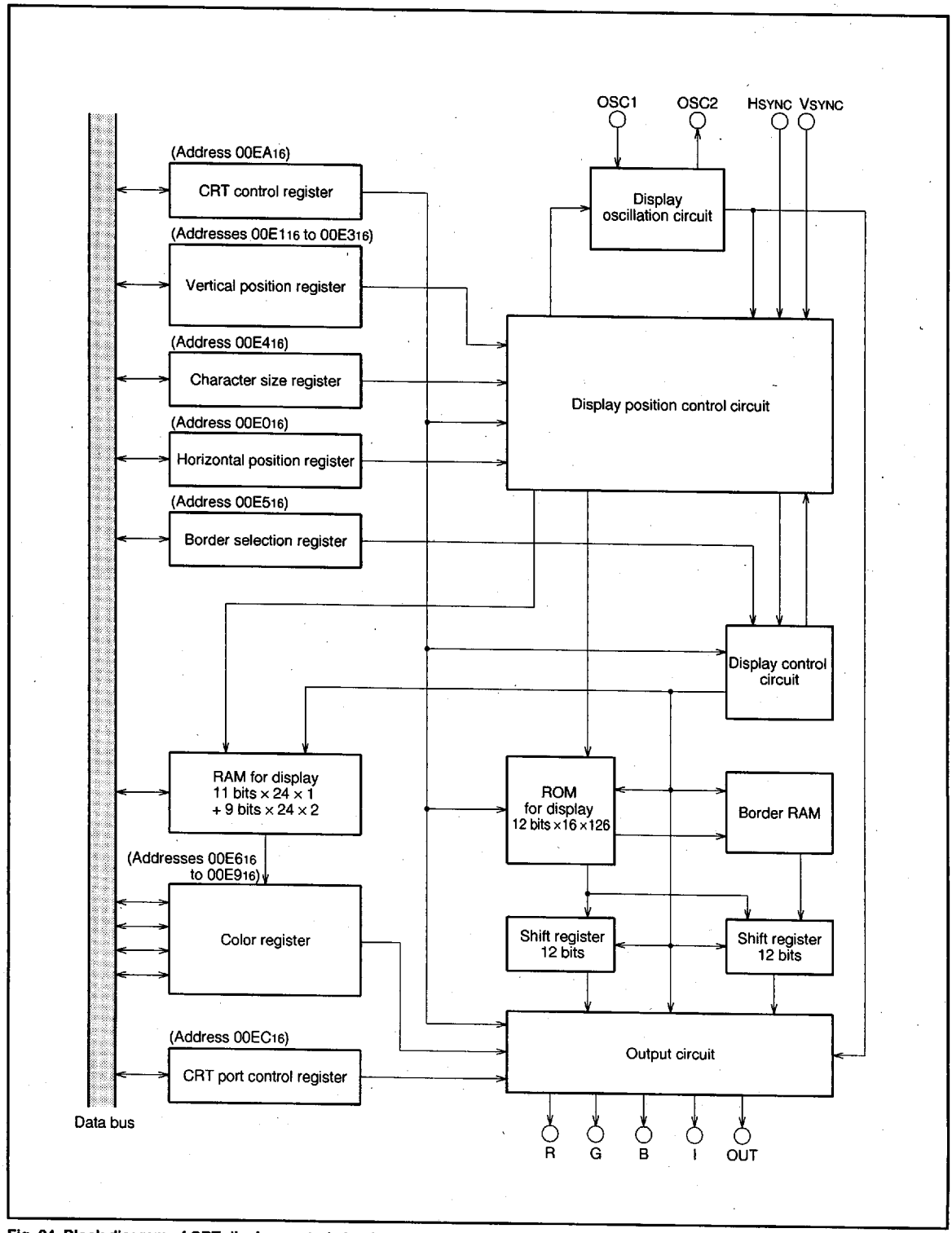


Fig. 24 Block diagram of CRT display control circuit

(2) Display Position

The display positions of characters are specified in units called a "block." There are three blocks, block 1 to block 3.

Up to 24 characters can be displayed in one block (refer to (4) Memory for Display).

The display position of each block in both horizontal and vertical directions can be set by software.

The horizontal direction is common to all blocks, and is selected from 64-step display positions in units of 4Tc (Tc=oscillating cycle for display).

The display position in the vertical direction is selected from 128-step display positions for each block in units of four scanning lines.

If the display start position of a block overlaps with some other block ((b) in Figure 27), a block of the smaller block No. (1 to 3) is displayed.

If when one block is displaying, some other block is displayed at the same display position ((c) in Figure 27), the former block is overridden and the latter is displayed.

The vertical position can be specified from 128-step positions (four scanning lines per step) for each block by setting values 00_{16} to $7F_{16}$ to bits 0 to 6 in the vertical position register (addresses $00E1_{16}$ to $00E3_{15}$). Figure 25 shows the structure of the vertical position register.

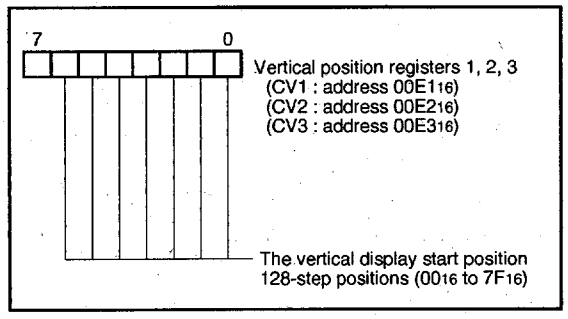


Fig. 25 Structure of vertical position registers

The horizontal direction is common to all blocks, and can be specified from 64-step display positions (4Tc per step (Tc=oscillation cycle for display) by setting values 00_{16} to $3F_{16}$ to bits 0 to 5 in the horizontal position register (address $00E0_{16}$). Figure 26 shows the structure of the horizontal position register.

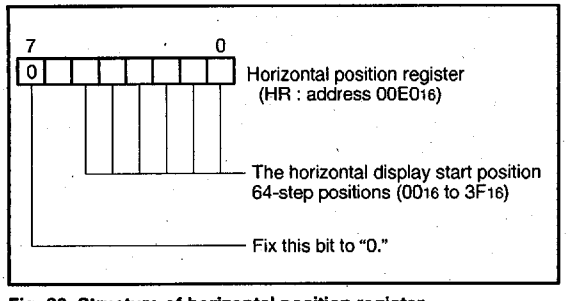
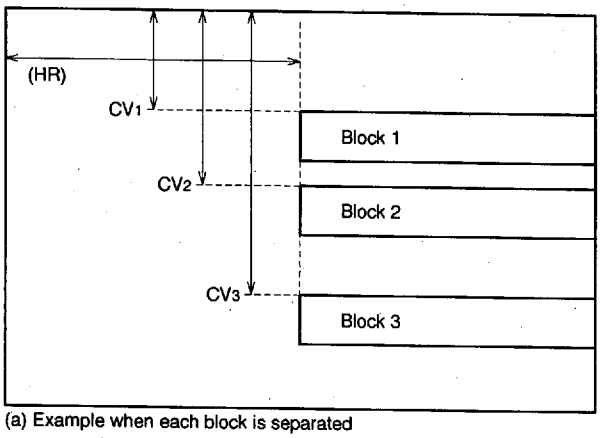
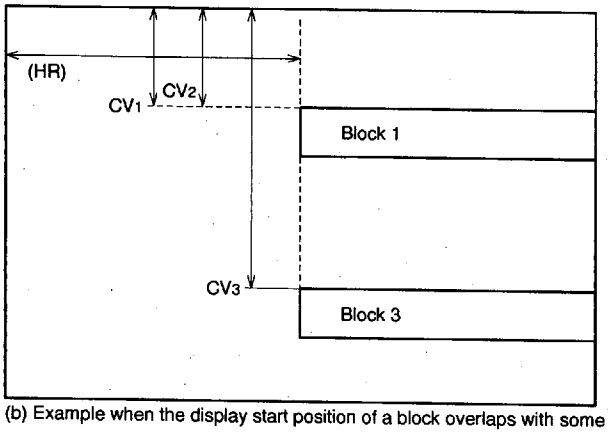


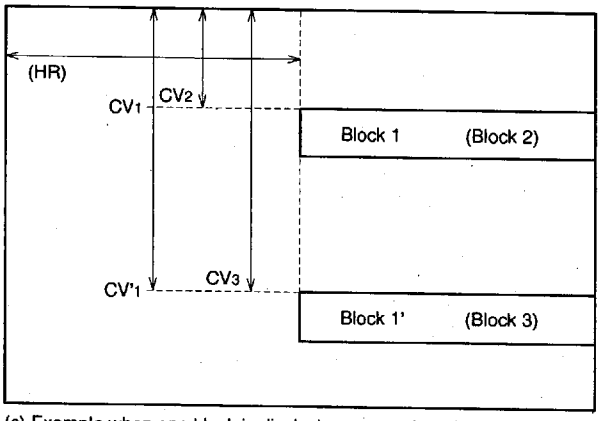
Fig. 26 Structure of horizontal position register



(a) Example when each block is separated



(b) Example when the display start position of a block overlaps with some other block



(c) Example when one block is displaying some other block is superimposed.

Fig. 27 Display position

(3) Character Size

The size of characters to be displayed can be selected from four sizes for each block. Use the character size register (address $00E4_{16}$) to set a character size. The character size in block 1 can be specified by using bits 0 and 1 in the character size register; the character size in block 2 can be specified by using bits 2 and 3; the character size in block 3 can be specified by using bits 4 and 5. Figure 28 shows the structure of the character size register.

The character size can be selected from four sizes: minimum size, medium size, large size, and extra large size. Each character size is determined by the number of scanning lines in the height (vertical) direction and the cycle of display oscillation (=Tc) in the width (horizontal) direction.

The small size consists of [one scanning line] × [1 Tc] ; the medium size consists of [two scanning lines] × [2 Tc]; the large size consists of [three scanning lines] × [3 Tc]; and the extra large size consists of [four scanning lines] × [4 Tc]. Table 5 shows the relationship between the set values in the character size register and the character sizes.

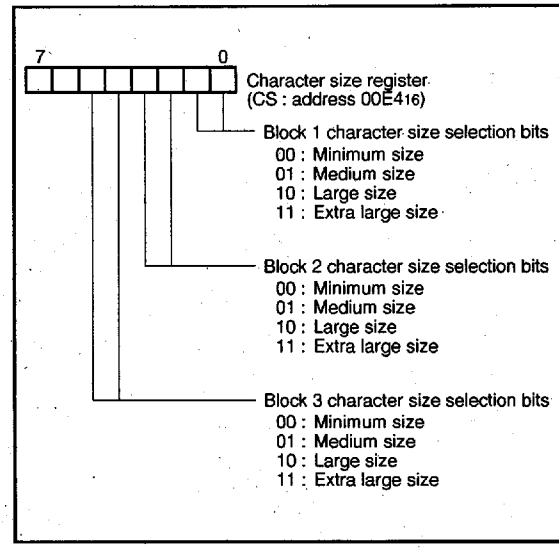


Fig. 28 Structure of character size register

Table 5. The relationship between the set values of the character size register and the character sizes

Set values of the character size register		Character size	Width (horizontal) direction Tc: oscillating cycle for display	Height (vertical) direction scanning lines
CS_{n1}	CS_{n0}			
0	0	Minimum	1 Tc	1
0	1	Medium	2 Tc	2
1	0	Large	3 Tc	3
1	1	Extra large	4 Tc	4

Note: The display start position in the horizontal direction is not affected by the character size. In other words, the horizontal display start position is common to all blocks even when the character size varies with each block (refer to Figure 29).

(4) Memory for Display

There are two types of memory for display : ROM of CRT display ROM (addresses 3000_{16} to $3FFF_{16}$) used to store character dot data (masked) and display RAM (addresses 2000_{16} to $20D7_{16}$) used to specify the colors of characters to be displayed. The following describes each type of display memory.

① ROM for display (addresses 3000_{16} to $3FFF_{16}$)

The CRT display ROM contains dot pattern data for characters to be displayed. For characters stored in this ROM to be actually displayed, it is necessary to specify them by writing the character code inherent to each character (code determined based on the addresses in the CRT display ROM) into the CRT display RAM.

The CRT display ROM has a capacity of 4K bytes. Because 32 bytes are required for one character data, the ROM can contain up to 128 kinds of characters. Actually, however, because two characters are required for test pattern use, the ROM can contain up to 126 kinds of characters for display use.

The CRT display ROM space is broadly divided into two areas. The [vertical 16 dots] × [horizontal (left side) 8 dots] data of display characters are stored in addresses 3000_{16} to $37FF_{16}$; the [vertical 16 dots] × [horizontal (right side) 4 dots] data of display characters are stored in addresses 3800_{16} to $3FFF_{16}$ (refer to Figure 30). Note however that the four upper bits in the data to be written to addresses 3800_{16} to $3FFF_{16}$ must be set to "1" (by writing data $F0_{16}$ to FF_{16}).

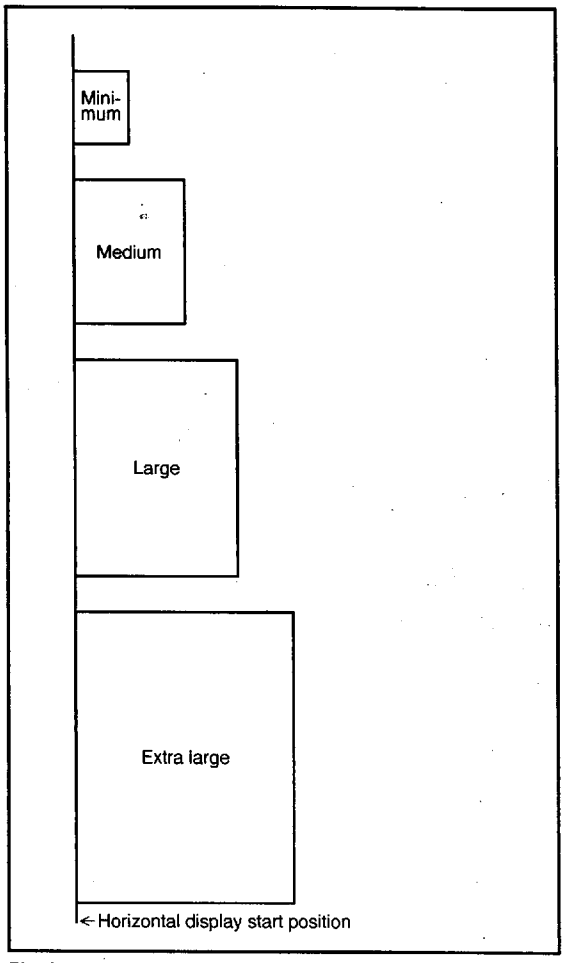


Fig. 29 Display start position of each character size (horizontal direction)

Table 6. Character code list

Character code	Contained up address of character data	
	Left 8 dots lines	Right 4 dots lines
00_{16}	3000_{16} to $300F_{16}$	3800_{16} to $380F_{16}$
01_{16}	3010_{16} to $301F_{16}$	3810_{16} to $381F_{16}$
02_{16}	3020_{16} to $302F_{16}$	3820_{16} to $382F_{16}$
03_{16} : 10_{16}	3030_{16} to $303F_{16}$: 3100_{16} to $310F_{16}$	3830_{16} to $383F_{16}$: 3900_{16} to $390F_{16}$
11_{16} : $4F_{16}$	3110_{16} to $311F_{16}$: $34F0_{16}$ to $34FF_{16}$	3910_{16} to $391F_{16}$: $3CF0_{16}$ to $3CFF_{16}$
50_{16} : $7D_{16}$	3500_{16} to $350F_{16}$: $37D0_{16}$ to $37DF_{16}$	$3D00_{16}$ to $3D0F_{16}$: $3FD0_{16}$ to $3FDF_{16}$
$7E_{16}$*	$37E0_{16}$ to $37EF_{16}$	$3FE0_{16}$ to $3FEF_{16}$
$7F_{16}$*	$37F0_{16}$ to $37FF_{16}$	$3FF0_{16}$ to $3FFF_{16}$

* For test pattern

The character code used to specify a character to be displayed is determined based on the address in the CRT display ROM in which that character is stored.
Assume that data for one character is stored at addresses $3XX0_{16}$ to $3XXF_{16}$ (XX denotes 00_{16} to $7F_{16}$) and addresses $3YY0_{16}$ to $3YYF_{16}$ (YY denotes 80_{16} to FF_{16}), then the character code for it is "XX_{16}".

In other words, character code for any given character is configured with two middle digits of the four-digit (hex-notated) addresses 3000_{16} to $37FF_{16}$ where data for that character is stored.
Table 6 lists the character codes.

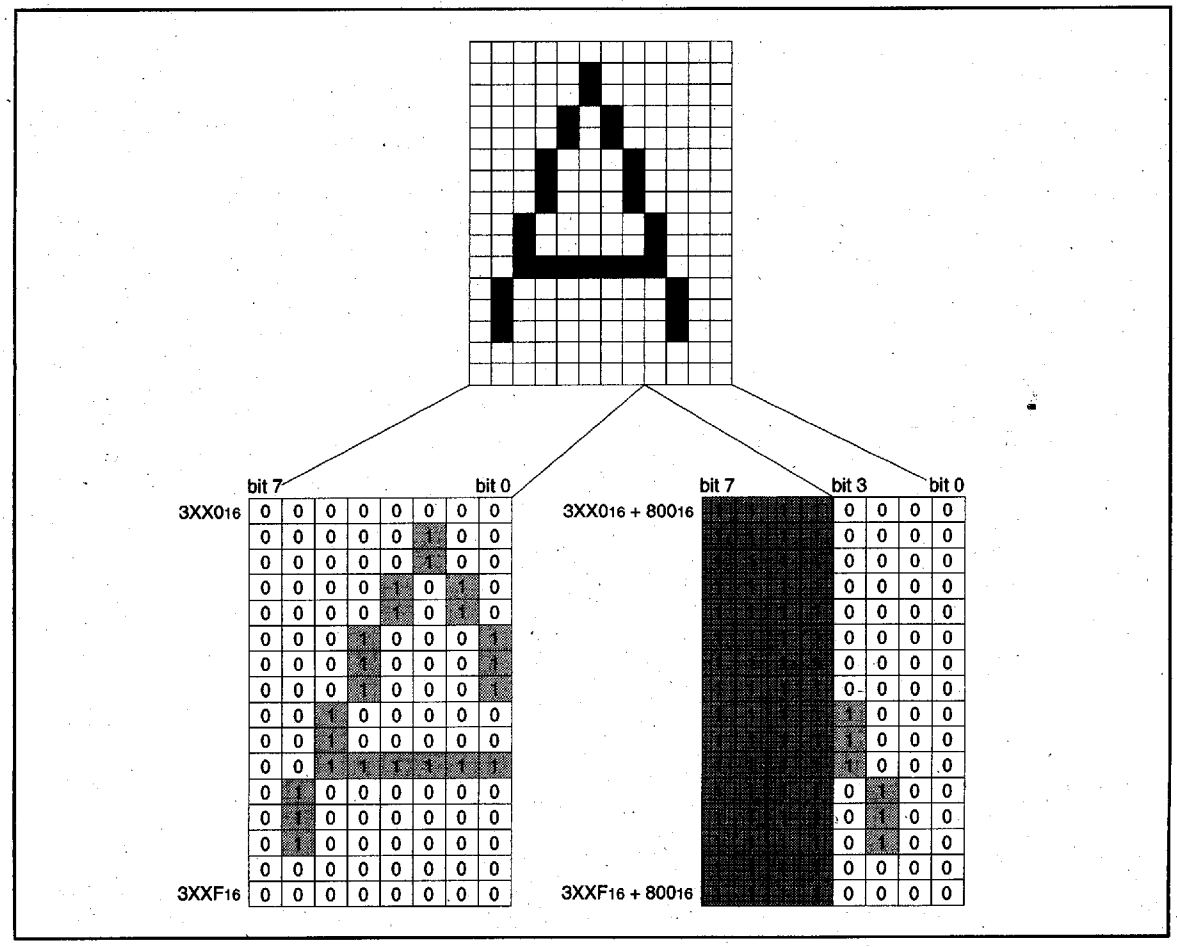


Fig. 30 Display character stored area

② RAM for display (2000_{16} to $20D7_{16}$)

The CRT display RAM is allocated at addresses 2000_{16} to $20D7_{16}$, and is divided into a display character code specifying part and display color specifying part for each block. Table 7 shows the contents of the CRT display RAM.

When a character is to be displayed at the first character (leftmost) position in block 1, for example, it is necessary to write the character code to the seven low-order bits (bits 0 to 6) in address 2000_{16} and the color register No. to the two low-order bits (bits 0 and 1) in address 2080_{16}. The color register No. to be written here is one of the four color registers in which the color to be displayed is set in advance. For details on color registers, refer to (5) Color Registers.

The structure of the CRT display RAM is shown in Figure 30. Write the character patterns at Table 8 and 9, when M37102M8-XXXSP is mask-ordered.

Table 7. The contents of the CRT display RAM

Block	Display position (from left)	Character code specification	Color specification
Block 1	1st character	2000_{16}	2080_{16}
	2nd character	2001_{16}	2081_{16}
	3rd character : 22nd character	2002_{16} : 2015_{16}	2082_{16} : 2095_{16}
	23rd character	2016_{16}	2096_{16}
	24th character	2017_{16}	2097_{16}
Not used		2018_{16} to $201F_{16}$	2098_{16} to $209F_{16}$
Block 2	1st character	2020_{16}	$20A0_{16}$
	2nd character	2021_{16}	$20A1_{16}$
	3rd character : 22nd character	2022_{16} : 2035_{16}	$20A2_{16}$: $20B5_{16}$
	23rd character	2036_{16}	$20B6_{16}$
	24th character	2037_{16}	$20B7_{16}$
Not used		2038_{16} to $203F_{16}$	$20B8_{16}$ to $20BF_{16}$
Block 3	1st character	2040_{16}	$20C0_{16}$
	2nd character	2041_{16}	$20C1_{16}$
	3rd character : 22nd character	2042_{16} : 2055_{16}	$20C2_{16}$: $20D5_{16}$
	23rd character	2056_{16}	$20D6_{16}$
	24th character	2057_{16}	$20D7_{16}$
Not used		2058_{16} to $207F_{16}$	

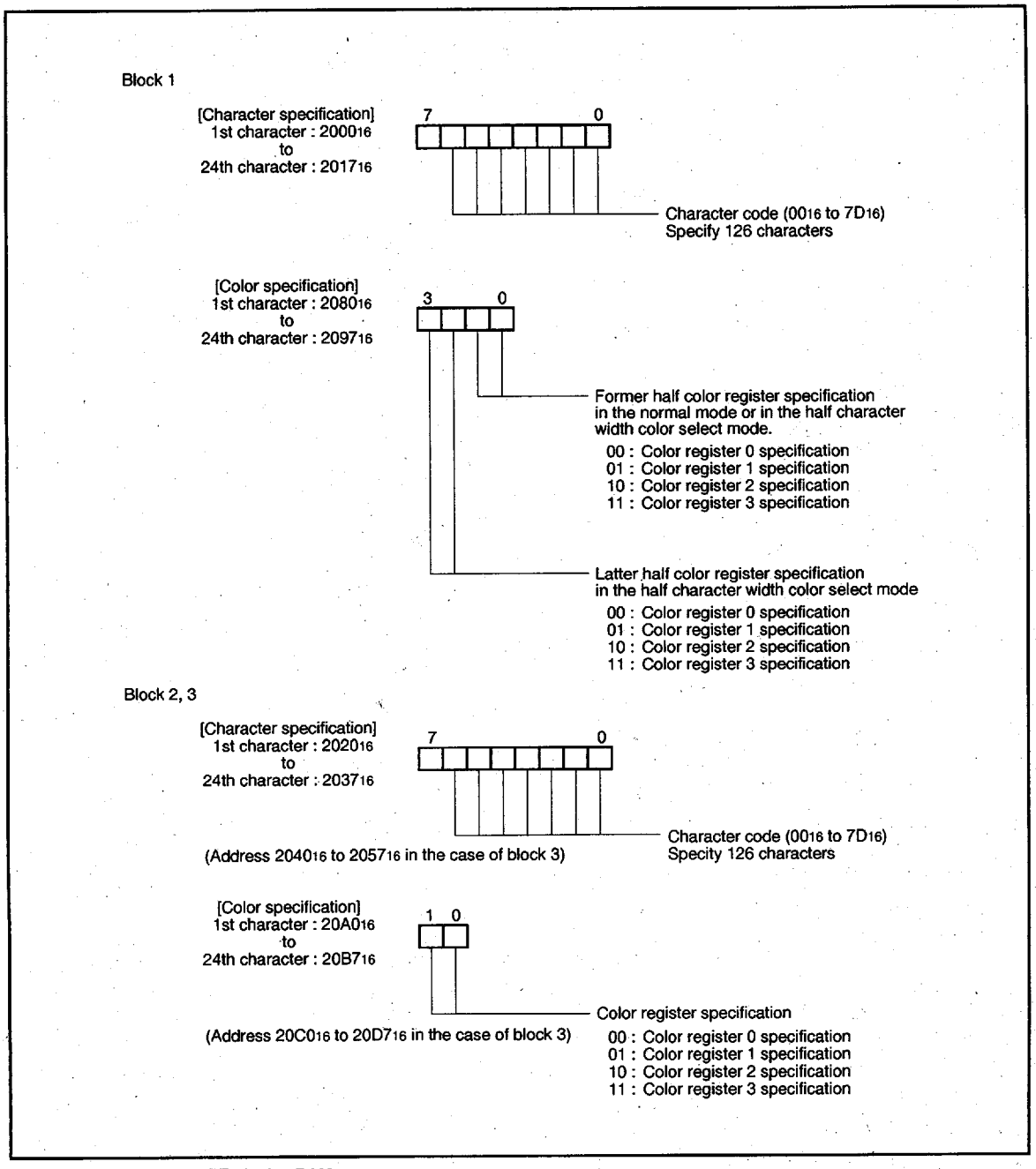


Fig. 31 Structure of the CRT display RAM

Table 8. Test character patterns 1

Address	Data	Address	Data
$37E0_{16}$	40_{16}	$3FE0_{16}$	$F0_{16}$
$37E1_{16}$	04_{16}	$3FE1_{16}$	$F0_{16}$
$37E2_{16}$	00_{16}	$3FE2_{16}$	$F4_{16}$
$37E3_{16}$	20_{16}	$3FE3_{16}$	$F0_{16}$
$37E4_{16}$	02_{16}	$3FE4_{16}$	$F0_{16}$
$37E5_{16}$	00_{16}	$3FE5_{16}$	$F2_{16}$
$37E6_{16}$	10_{16}	$3FE6_{16}$	$F0_{16}$
$37E7_{16}$	01_{16}	$3FE7_{16}$	$F0_{16}$
$37E8_{16}$	80_{16}	$3FE8_{16}$	$F0_{16}$
$37E9_{16}$	08_{16}	$3FE9_{16}$	$F0_{16}$
$37EA_{16}$	00_{16}	$3FEA_{16}$	$F8_{16}$
$37EB_{16}$	40_{16}	$3FEB_{16}$	$F0_{16}$
$37EC_{16}$	04_{16}	$3FEC_{16}$	$F0_{16}$
$37ED_{16}$	00_{16}	$3FED_{16}$	$F4_{16}$
$37EE_{16}$	20_{16}	$3FEE_{16}$	$F0_{16}$
$37EF_{16}$	02_{16}	$3FEF_{16}$	$F0_{16}$

Table 9. Test character patterns 2

Address	Data	Address	Data
$37F0_{16}$	00_{16}	$3FF0_{16}$	$F0_{16}$
$37F1_{16}$	00_{16}	$3FF1_{16}$	$F0_{16}$
$37F2_{16}$	00_{16}	$3FF2_{16}$	$F0_{16}$
$37F3_{16}$	00_{16}	$3FF3_{16}$	$F0_{16}$
$37F4_{16}$	00_{16}	$3FF4_{16}$	$F0_{16}$
$37F5_{16}$	00_{16}	$3FF5_{16}$	$F0_{16}$
$37F6_{16}$	00_{16}	$3FF6_{16}$	$F0_{16}$
$37F7_{16}$	00_{16}	$3FF7_{16}$	$F0_{16}$
$37F8_{16}$	00_{16}	$3FF8_{16}$	$F0_{16}$
$37F9_{16}$	00_{16}	$3FF9_{16}$	$F0_{16}$
$37FA_{16}$	00_{16}	$3FFA_{16}$	$F0_{16}$
$37FB_{16}$	00_{16}	$3FFB_{16}$	$F0_{16}$
$37FC_{16}$	00_{16}	$3FFC_{16}$	$F0_{16}$
$37FD_{16}$	00_{16}	$3FFD_{16}$	$F0_{16}$
$37FE_{16}$	00_{16}	$3FFE_{16}$	$F0_{16}$
$37FF_{16}$	00_{16}	3FFF16	$F0_{16}$

(5) Color Registers

The color of a displayed character can be specified by setting the color to one of the four color registers (CO0 to CO3: addresses $00E6_{16}$ to $00E9_{16}$) and then specifying that color register with the CRT display RAM.

There are four color outputs: R, G, B, and I. By using a combination of these outputs, it is possible to set $2^4 - 1$ (when no output) = 15 colors. However, because only four color registers are available, up to four colors can be displayed at one time.

R, G, B, and I outputs are set by using bits 0 to 3 in the color register. Bit 4 in the color register is used to set a character or blank output; bit 5 is used to specify whether a character output or blank output. Figure 32 shows the structure of the color register.

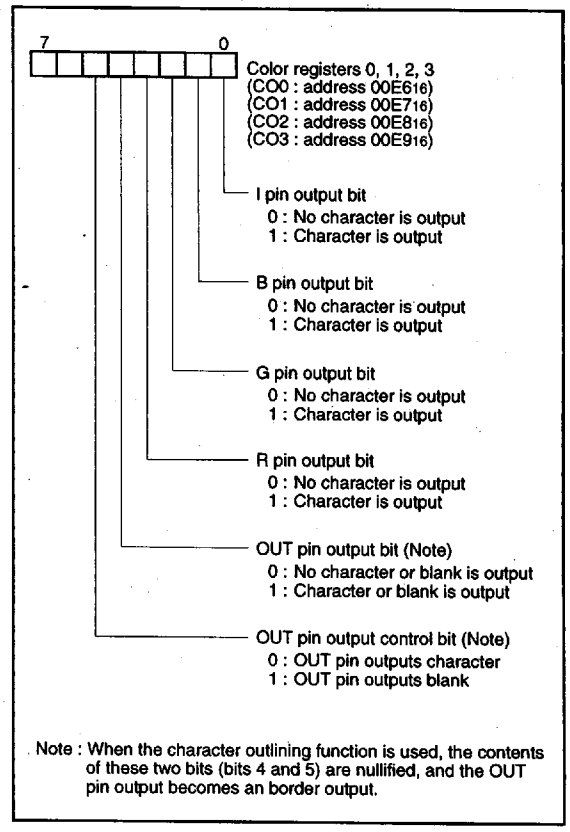


Fig. 32 Structure of color registers

(6) 1/2-Character Unit Color Specification Mode

By setting "1" to bit 4 in the CRT control register (address $00EA_{16}$) it is possible to specify colors in units of a half character size (vertical 16 dots × horizontal 6 dots) for characters in block 1 only.
In the half character width color select mode, colors of display characters in block 1 are specified as follows:

① The left half of the character is set to the color of the color register that is specified by bits 0 and 1 at the color register specifying addresses in the CRT display RAM (addresses 2080_{16} to 2097_{16}).
② The right half of the character is set to the color of the color register that is specified by bits 2 and 3 at the color register specifying address in the CRT display RAM (addresses 2080_{16} to 2097_{16}).

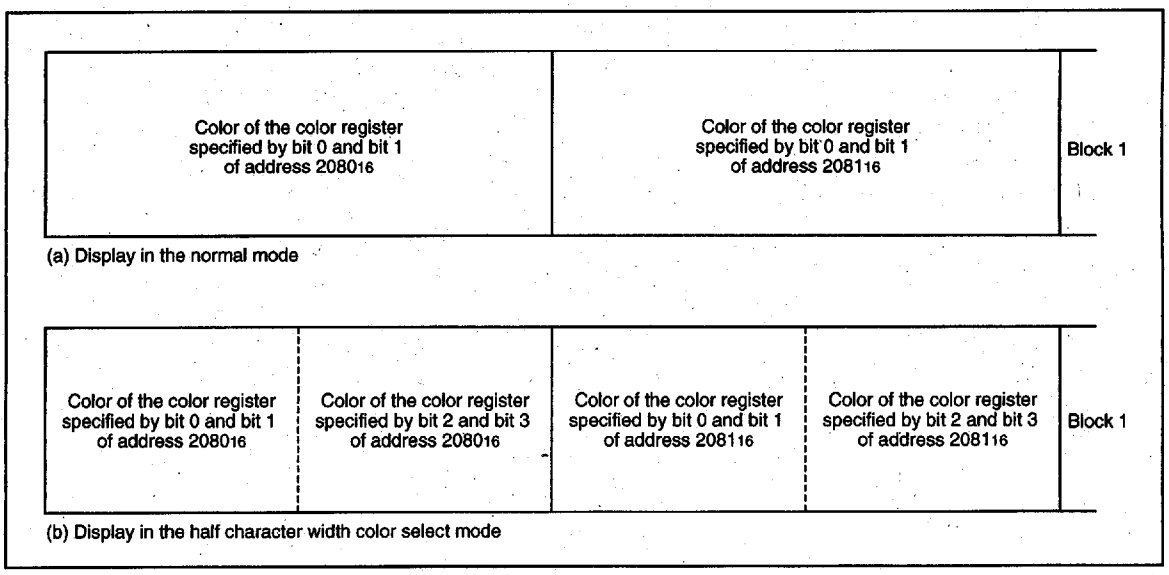


Fig. 33 Difference between normal color select mode and 1/2-character unit color specification mode

(7) Multiline Display

The M37102M8-XXXSP can normally display three lines on the CRT screen by displaying three blocks at different vertical positions. In addition, it allows up to 16 lines to be displayed by using a CRT interrupt and display block counter.

The CRT interrupt works in such a way that when display of one block is terminated, an interrupt request is generated.

In other words, character display for a certain block is initiated when the scanning line reaches the display position for that block (specified with vertical and horizontal position registers) and when the range of that block is exceeded, an interrupt is applied.

The display block counter is used to count the number of blocks that have just been displayed. Each time the display of one block is terminated, the contents of the counter are incremented by one.

For multiline display, it is necessary to enable the CRT interrupt (by clearing the interrupt disable flag to "0" and setting the CRT interrupt enable bit (bit 4 at address $00FE_{16}$) to "1"), then execute the following processing in the CRT interrupt handling routine.

① Read the value of the display block counter.
② The block for which display is terminated (i.e., the cause of CRT interrupt generation) can be determined by the value read in ①.
③ Replace the display character data and vertical display position of that block with the character data (contents of CRT display RAM) and vertical display position (contents of vertical position register) to be displayed next.

Figure 34 shows the structure of the display block counter.

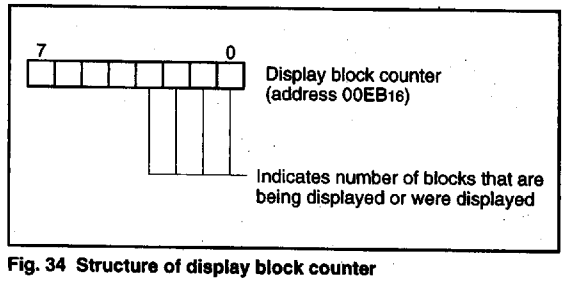


Fig. 34 Structure of display block counter

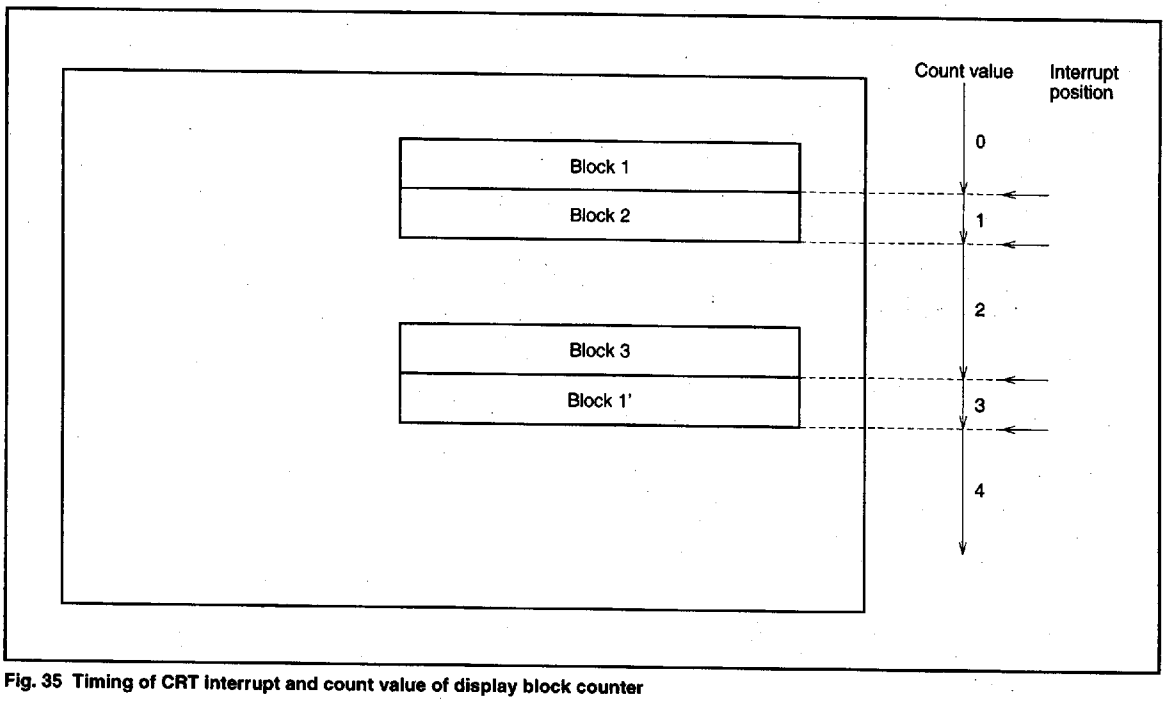


Fig. 35 Timing of CRT interrupt and count value of display block counter

(8) Scanning Line Double Count Mode

One dot in a displayed character is normally shown by one scanning line. In the scanning line double count mode, one dot can be shown by two scanning lines. As a result, the displayed dot is extended two times the normal size in the vertical direction only. (That is to say, the height of a character is extended twofold.)

In addition, because the scanning line count is doubled, the display start position of a character is also extended two-fold in the vertical direction. In other words, whereas the contents set in the vertical position register in the normal mode are 128 steps from 00_{16} to $7F_{16}$, or four scanning lines per step, the number of steps in the scanning line double count mode is 64 from 00_{16} to $3F_{16}$, or eight scanning lines per step.

If the contents of the vertical position register for a block are set in the address range of 40_{16} to $7F_{16}$ in the scanning line double count mode, that block cannot be displayed (not output to the CRT screen).

In the scanning line double count mode can be specified by setting bit 6 in the CRT control register (address $00EA_{16}$) to "1".

Because this function works in units of screen, even when the mode is changed the mode about the scanning line count during display of one screen, the double count mode only becomes valid from the time the next screen is displayed.

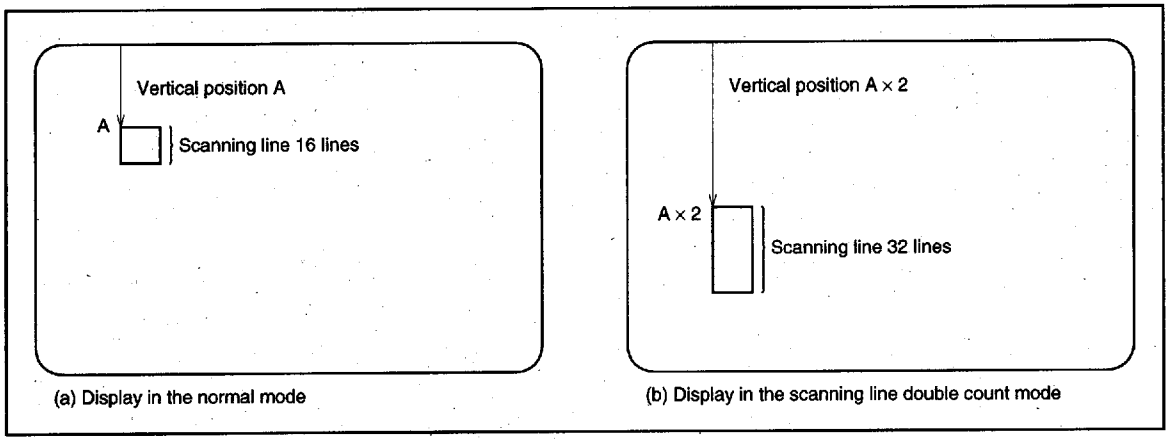


Fig. 36 Display in the normal mode and in the scanning line double count mode

(9) Character Border Function

An border of a one clock (one dot) equivalent size can be added to a character to be displayed in both horizontal and vertical directions. The border is output from the OUT pin. In this case, bits 4 and 5 in the color register (contents output from the OUT pin) are nullified, and the border is output from the OUT pin instead.

Border can be specified in units of block by using the border select register (address $00E5_{16}$). Table 10 shows the relationship between the values set in the border select register and the character border function. Figure 38 shows the structure of the border select register.

Table 10. The relationship between the value set in the border selection register and the character border function

Border selection register		Functions	Example of output
MDn1	MDn0		
X	0	Ordinary	R, G, B, I output OUT output
0	1	Border including character	R, G, B, I output OUT output
1	1	Border not including character	R, G, B, I output OUT output

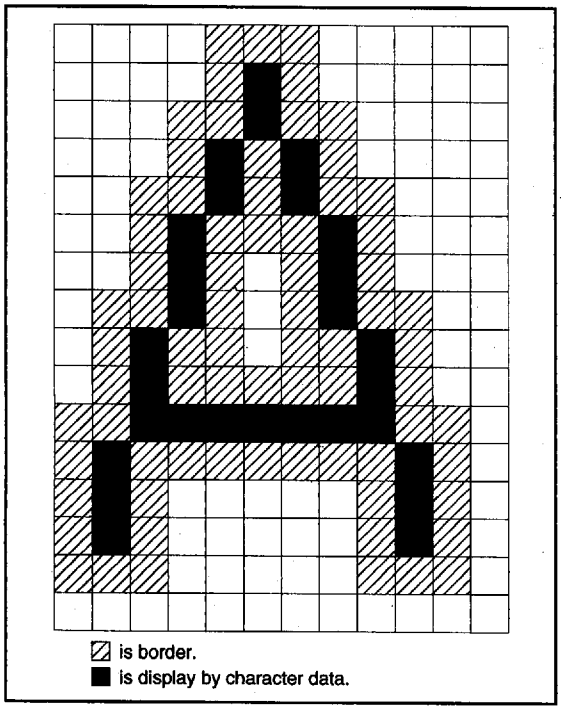


Fig. 37 Example of border

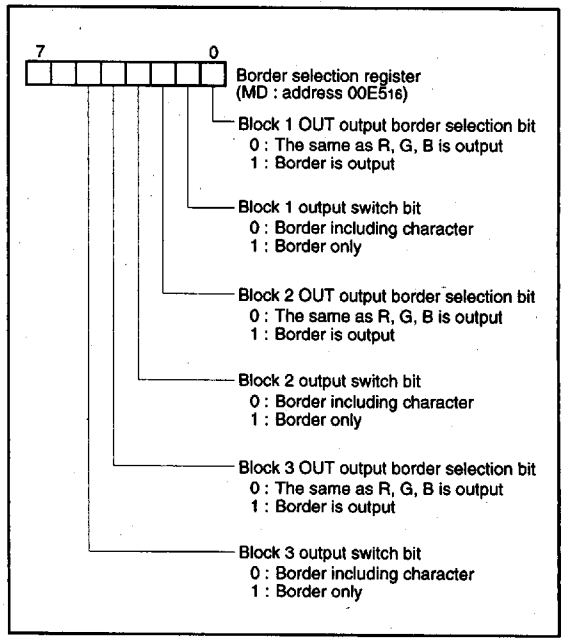


Fig. 38 Structure of border selection register

(10) CRT Output Pin Control

CRT output pins R, G, B, I, and OUT are respectively shared with port $P5_2$, $P5_3$, $P5_4$, $P5_5$, and $P5_6$. When the corresponding bits in the port P5 control register (address $00CB_{16}$) are cleared to "0", the pins are set for CRT output; when the bits are set to "1", the pins function as port P5 (general-purpose output pins).

The polarities of CRT outputs (R, G, B, I, and OUT, as well as H_{SYNC} and V_{SYNC}) can be specified by using the CRT port control register (address $00EC_{16}$).

Use bits 0 to 4 in the CRT port control register to set the output polarities of H_{SYNC}, V_{SYNC}, R/G/B, I, and OUT. When these bits are cleared to "0", a positive polarity is selected; when the bits are set to "1", a negative polarity is selected.

Bits 5 to 7 in the CRT port control register are used to specify pin by pin whether normal video signals or R-MUTE, G-MUTE, and B-MUTE signals are output from each pin (R, G, B). When set for R-MUTE, G-MUTE, and B-MUTE outputs, the whole background colors of the screen become red, green, and blue.

Figure 39 shows the structure of the CRT port control register.

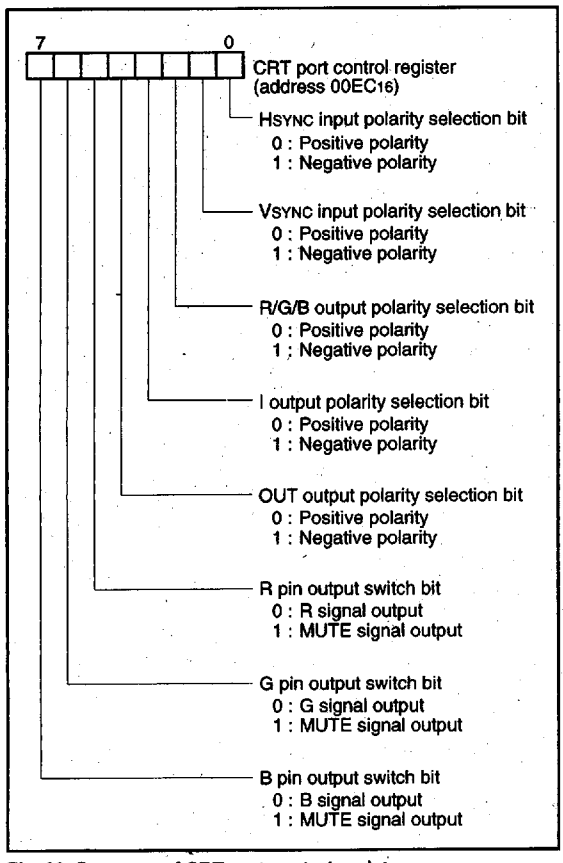


Fig. 39 Structure of CRT port control register

(11) Wipe Function

① Wipe mode

The M37102M8-XXXSP/FP allows the display area to be gradually expanded or shrunk in the vertically direction in units of 1H (H: H_{SYNC} signal). There are three modes for this wipe method. Each mode has Down and UP modes, providing a total of six modes.

Table 11 shows the contents of each scroll mode.

② Wipe speed

The scroll speed is determined by the vertical synchronization (V_{SYNC}) signal. For the NTSC interlace method, assuming that

V=16.7ms 262.5 H_{SYNC} signals per screen

we obtain the scroll speed as shown in Table 12.

Wipe resolution varies with each wipe mode. In mode 1 and mode 2, one of three resolutions (1H, 2H, 4H) can be selected. In mode 3, wipe is done in units of 4H alone.

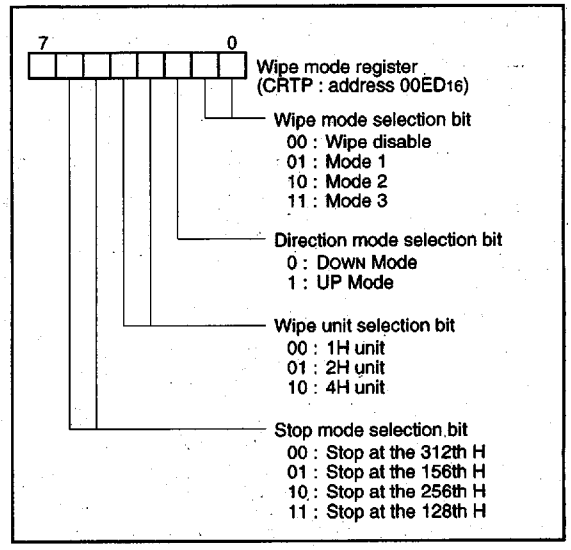


Fig. 40 Structure of wipe mode register

Table 11. Wipe operation in each mode and the values of wipe mode register

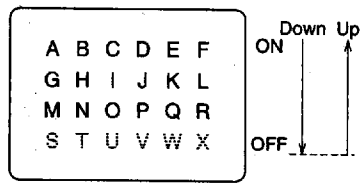
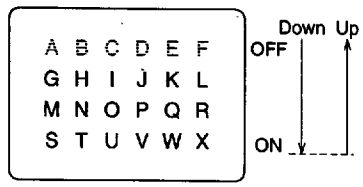
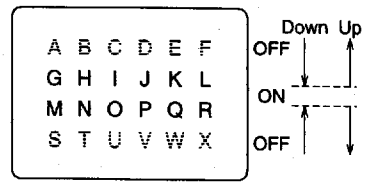
Mode		Wipe operation		Wipe mode register		
				Bit 2	Bit 1	Bit 0
1	DOWN	Appear from upper side		0	0	1
	UP	Erase from lower side		1	0	1
2	DOWN	Erase from upper side		0	1	0
	UP	Appear from lower side		1	1	0
3	DOWN	Erase from both upper and lower side		0	1	1
	UP	Appear to both upper and lower side		1	1	1

Table 12. Wipe speed

Wipe resolution	Wipe speed (in all picture)
1 H unit	16.7 (ms) × 262.5÷1=4 (s)
2 H unit	16.7 (ms) × 262.5÷2=2 (s)
4 H unit	16.7 (ms) × 262.5÷4=1 (s)

Table 13. Wipe mode and wipe resolution

Mode	Wipe resolution	Wipe speed
Mode 1 Mode 2	1 H Unit	about 4 second
	2 H Unit	about 2 second
	4 H Unit	about 1 second
Mode 3	4 H Unit	about 1 second

INTERRUPT INTERVAL DETERMINATION FUNCTION

The M37102M8-XXXSP/FP incorporates an interrupt interval determination circuit. This interrupt interval determination circuit has an 8-bit binary up counter as shown in Figure 41.

Using this counter, it determines an interval on the INT1 or INT2 (refer to Figure 43).

The following describes how the interrupt interval is determined.

1. The interrupt input to be determined (INT1 input or INT2 input) is selected by using bit 2 in the interrupt interval determination control register (address 00D816). When this bit is cleared to "0", the INT1 input is selected; when the bit is set to "1", the INT2 input is selected.
2. When the INT1 input is to be determined, the polarity is selected by using bit 3 of the interrupt interval determination control register; when the INT2 input is to be determined, the polarity is selected by using bit 4 of the interrupt interval determination control register.
   When the relevant bit is cleared to "0", determination is made of the interval of a positive polarity (rising transition); when the bit is set to "1", determination is made of the interval of a negative polarity (falling transition).
3. The reference clock is selected by using bit 1 of the interrupt interval determination control register. When the bit is cleared to "0", a 64μs clock is selected; when the bit is set to "1", a 32μs clock is selected (based on an oscillation frequency of 4MHz in either case).
4. Simultaneously when the input pulse of the specified polarity (rising or falling transition) occurs on the INT1 pin (or INT2 pin), the 8-bit binary up counter starts counting up with the selected reference clock (64μs or 32μs).
5. Simultaneously with the next input pulse, the value of the 8-bit binary up counter is loaded into the determination register (address $00D7_{16}$) and the counter is immediately reset (00_{16}). The reference clock is input in succession even after the counter is reset, and the counter restarts counting up from "00_{16}".
6. When count value "FE_{16}" is reached, the 8-bit binary up counter stops counting. Then, simultaneously when the next reference clock is input, the counter sets value "FF_{16}" to the determination register.

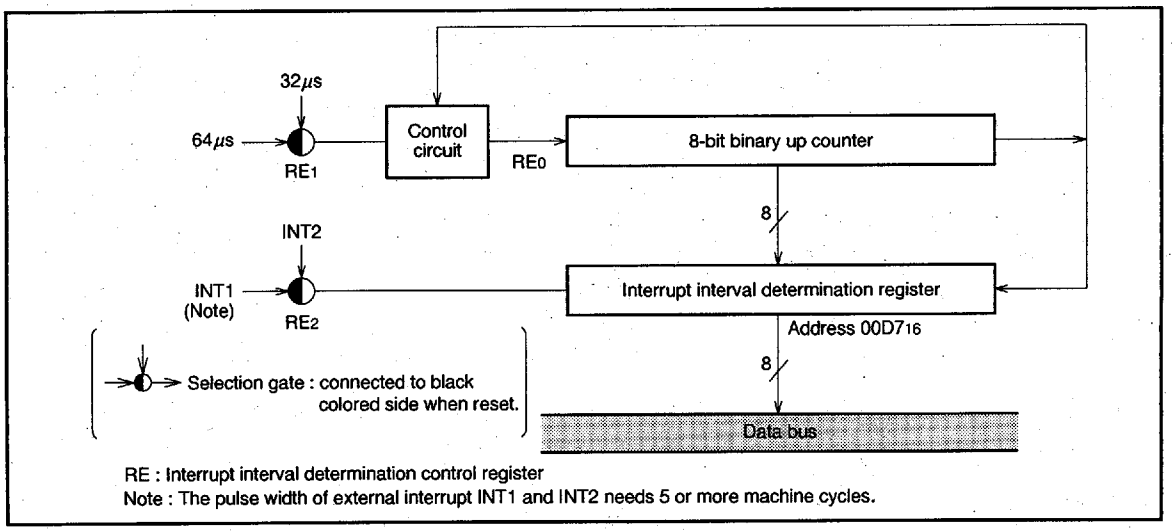


Fig. 41 Block diagram of interrupt interval determination circuit

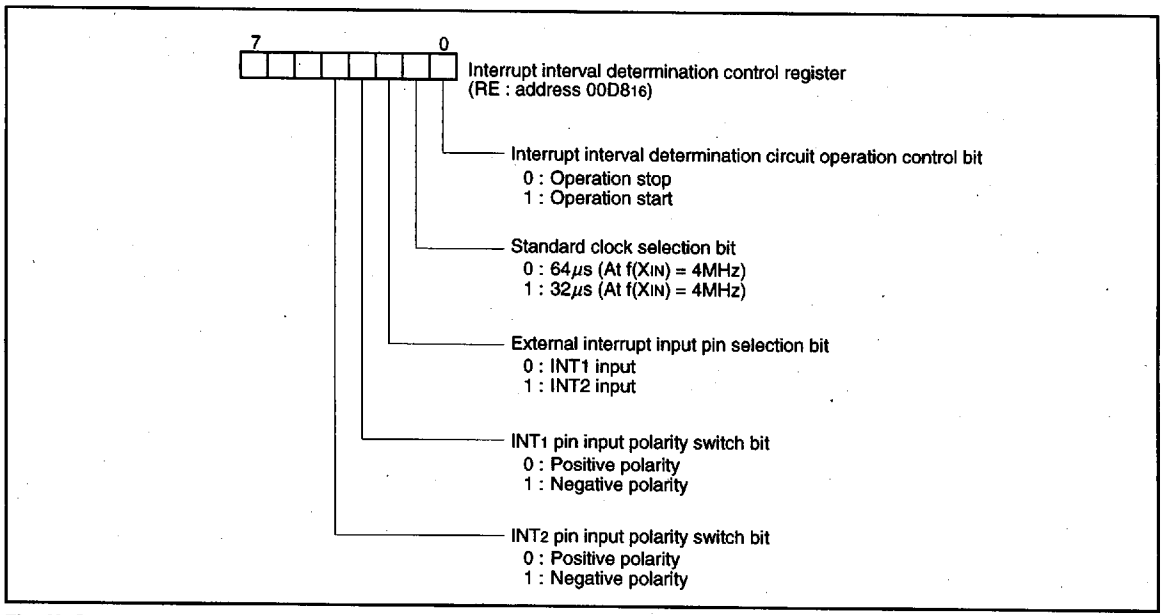


Fig. 42 Structure of interrupt space distinguish control register

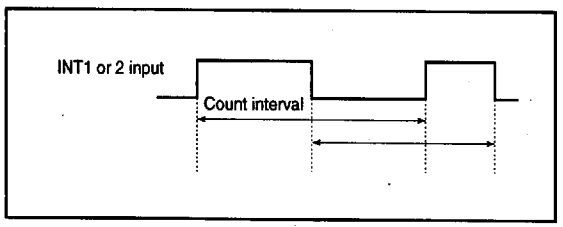


Fig. 43 Measuring interval

RESET CIRCUIT

The M37102M8-XXXSP/FP is reset according to the sequence shown in Figure 46. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for no less than 2μs while the power voltage is 5V±10% and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 44.

An example of the reset circuit is shown in Figure 45. The reset input voltage must be kept below 0.6V until the supply voltage surpasses 4.5V.

		Address	
(1)	Port P0 directional register	($00C1_{16}$)···	00_{16}
(2)	Port P1 directional register	($00C3_{16}$)···	00_{16}
(3)	Port P2 directional register	($00C5_{16}$)···	00_{16}
(4)	Port P3 directional register	($00C7_{16}$)···	0 0 0 0 0 0 0
(5)	Port P4 directional register	($00C9_{16}$)···	00_{16}
(6)	Port P5 control register	($00CB_{16}$)···	0 0 0 0 0
(7)	Port P6 directional register	($00CD_{16}$)···	00_{16}
(8)	PWM output control register 1	($00D5_{16}$)···	00_{16}
(9)	PWM output control register 2	($00D6_{16}$)···	0 0 0 0 0
(10)	Interrupt interval determination register	($00D7_{16}$)···	00_{16}
(11)	Interrupt interval determination control register	($00D8_{16}$)···	0 0 0 0 0
(12)	Special mode register 1	($00DA_{16}$)···	00_{16}
(13)	Special mode register 2	($00DB_{16}$)···	00_{16}
(14)	Serial I/O1 mode register	($00DC_{16}$)···	0 0 0 0 0 0
(15)	Serial I/O2 mode register	($00DE_{16}$)···	0 0 0 0 0 0
(16)	Horizontal position register	($00E0_{16}$)···	0 0 0 0 0 0 0
(17)	Color register 0	($00E6_{16}$)···	0 0 0 0 0 0
(18)	Color register 1	($00E7_{16}$)···	0 0 0 0 0 0
(19)	Color register 2	($00E8_{16}$)···	0 0 0 0 0 0
(20)	Color register 3	($00E9_{16}$)···	0 0 0 0 0 0
(21)	CRT control register	($00EA_{16}$)···	00_{16}
(22)	Display block counter	($00EB_{16}$)···	0 0 0 0
(23)	CRT port control register	($00EC_{16}$)···	00_{16}
(24)	Wipe control register	($00ED_{16}$)···	0 0 0 0 0 0 0
(25)	A-D control register	($00EF_{16}$)···	0 0 0 0 0
(26)	Timer 1	($00F0_{16}$)···	FF_{16}
(27)	Timer 2	($00F1_{16}$)···	07_{16}
(28)	Timer 3	($00F2_{16}$)···	FF_{16}
(29)	Timer 4	($00F3_{16}$)···	07_{16}
(30)	Timer 12 mode register	($00F4_{16}$)···	0 0 0 0 0
(31)	Timer 34 mode register	($00F5_{16}$)···	0 0 0 0 0
(32)	CPU mode register	($00FB_{16}$)···	1 1 1 1 1 1 0 0
(33)	Interrupt request register 1	($00FC_{16}$)···	0 0 0 0 0 0
(34)	Interrupt request register 2	($00FD_{16}$)···	0 0 0 0 0
(35)	Interrupt control register 1	($00FE_{16}$)···	0 0 0 0 0 0
(36)	Interrupt control register 2	($00FF_{16}$)···	0 0 0 0 0
(37)	Processor status register	(PS)···	1
(38)	Program counter	(PCH)···	Contents of address $FFFF_{16}$
		(PCL)···	Contents of address $FFFE_{16}$

Note : The blank above, the contents of all other registers and RAM are undefined, so set their initial values.
At reset, "0" is read from all bits which is not used.

Fig. 44 Internal state at reset

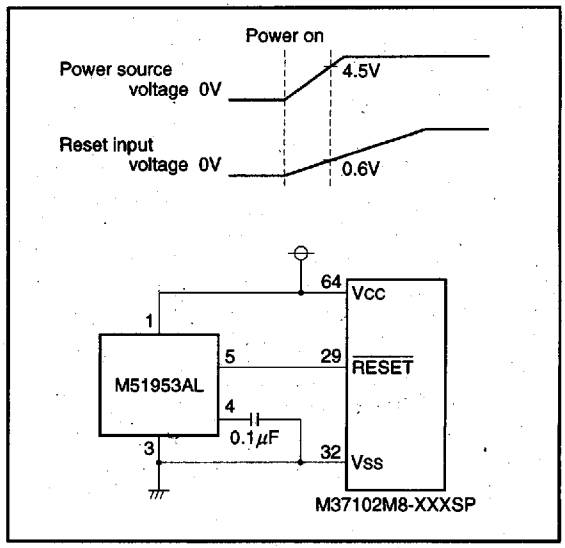


Fig. 45 Example of reset circuit

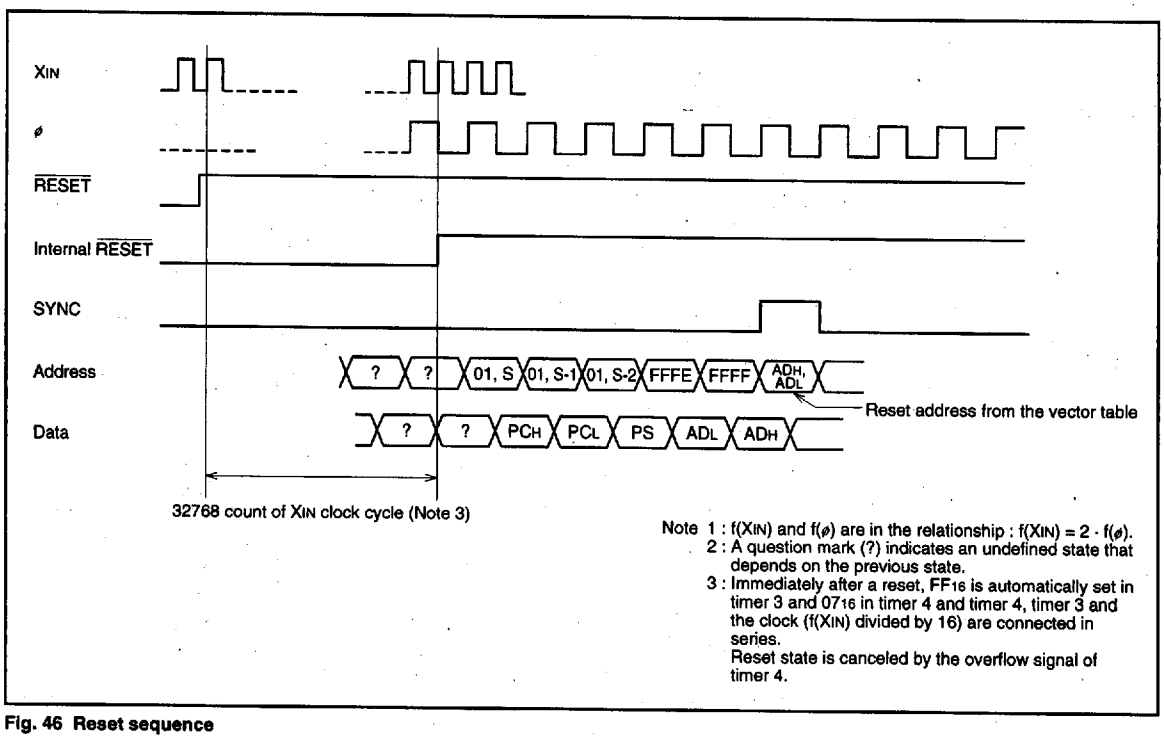


Fig. 46 Reset sequence

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 3), port P0 can be accessed at zero page memory address $00C0_{16}$.

Port P0 has a directional register (address $00C1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down.

Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

(2) Port P1

Port P1 has the same function as port P0.

(3) Port P2

Port P2 has the same function as port P0.

(4) Port P3

Port P3 is an 7-bit I/O port with function similar to port P0, but the output structure of $P3_0$, $P3_1$ is CMOS output and $P3_2$-$P3_6$ is N-channel open drain.

$P3_2$, $P3_3$ are in common with the external clock input pins of timer 2 and 3.

$P3_4$, $P3_6$ are in common with the external interrupt input pins INT1, INT2 and $P3_5$, $P3_6$ with the analog input pins of A-D comparator A-D1, A-D2.

(5) Port P4

Port P4 is an 8-bit I/O port with function similar to port P0, but the output structure is N-channel open drain output.

All pins have program selectable dual functions. When a serial I/O1 function is selected, $P4_0$-$P4_3$ work as input/output pins of serial I/O1. When a serial I/O2 function is selected, $P4_4$-$P4_7$ work as input/output pins of serial I/O2.

In the special serial I/O mode, $P4_4$, $P4_5$ work as SDA, SCL pins. $P4_6$, $P4_7$ are in common with PWM8 and 9 output pins.

(6) OSC1, OSC2 pins

Clock input/output pins for CRT display function.

(7) H_{SYNC}, V_{SYNC} pins

H_{SYNC} is a horizontal synchronizing signal input pin for CRT display.

V_{SYNC} is a vertical synchronizing signal input pin for CRT display.

(8) R, G, B, I, OUT pins

This is an 5-bit output pin for CRT display and in common with $P5_2$-$P5_6$.

(9) Port P6

Port P6 is an 8-bit I/O port with function similar to port P0, but the output structure is N-channel open drain output.

This port is in common with 8-bit PWM output pin PWM0-PWM7.

(10) D-A pin

This is a 14-bit PWM output pin.

(11) ϕ pin

The internal system clock (1/4 the frequency of the oscillator connected between the X_{IN} and X_{OUT} pins) is output from this pin. If an STP or WIT instruction is executed, output stops after going "H".

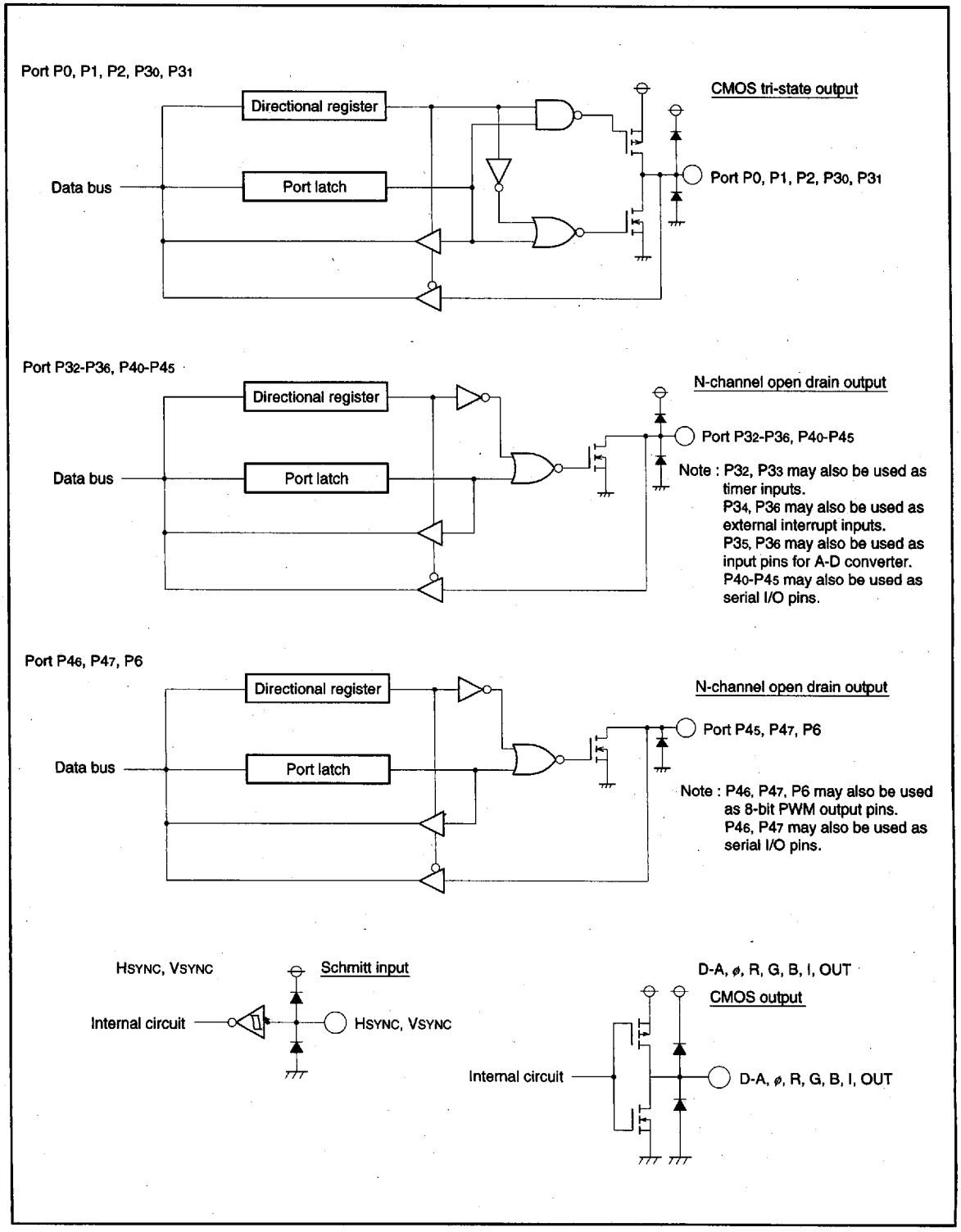


Fig. 47 I/O pin block diagram

CLOCK GENERATING CIRCUIT

The built-in clock generating circuit is shown in Figure 50.

When the STP instruction is executed, the internal clock ø stops oscillating at "H" level. At the same time, timers 3 and 4 are connected in hardware and "FF_{16}" is set in the timer 3, "07_{16}" is set in the timer 4. Select f(X_{IN})/16 as the timer 3 count source (set bit 0 of the timer 34 mode register to "0" before the execution of the STP instruction). And besides, set the timer 3 and timer 4 interrupt enable bits to disabled ("0") before execution of the STP instruction.

The oscillator is restarted when an interrupt is accepted. However, the clock ø keeps its "H" level until timer 4 overflows.

This is because the oscillator needs a set-up period if a ceramic resonator or a quartz-crystal oscillator is used.

When the WIT instruction is executed, the internal clock ø stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted (Note). Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait state, set the interrupt enable bit to "1" before executing the STP or the WIT instruction.

Note: In the wait mode, the following interrupts are invalid.

(1) V_{SYNC} interrupt
(2) CRT interrupt
(3) Timer 2 interrupt using $P3_2$/TIM2 pin input as count source
(4) Timer 3 interrupt using $P3_3$/TIM3 pin input as count source
(5) Timer 4 interrupt using f(X_{IN})/2 as count source

The circuit example using a ceramic resonator (or a quartz-crystal oscillator) is shown in Figure 48.

Use the circuit constants in accordance with the resonator manufacturer's recommended values.

The example of external clock usage is shown in Figure 49 X_{IN} is the input, and X_{OUT} is open.

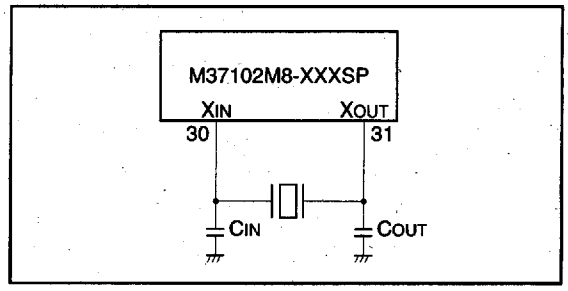


Fig. 48 Ceramic resonator circuit example

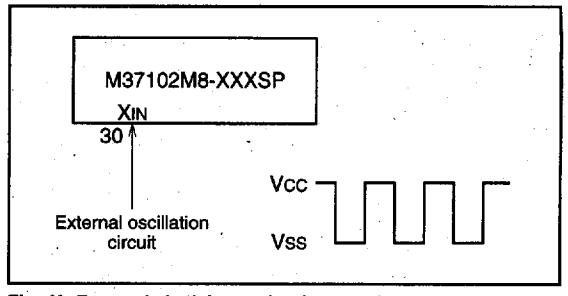


Fig. 49 External clock input circuit example

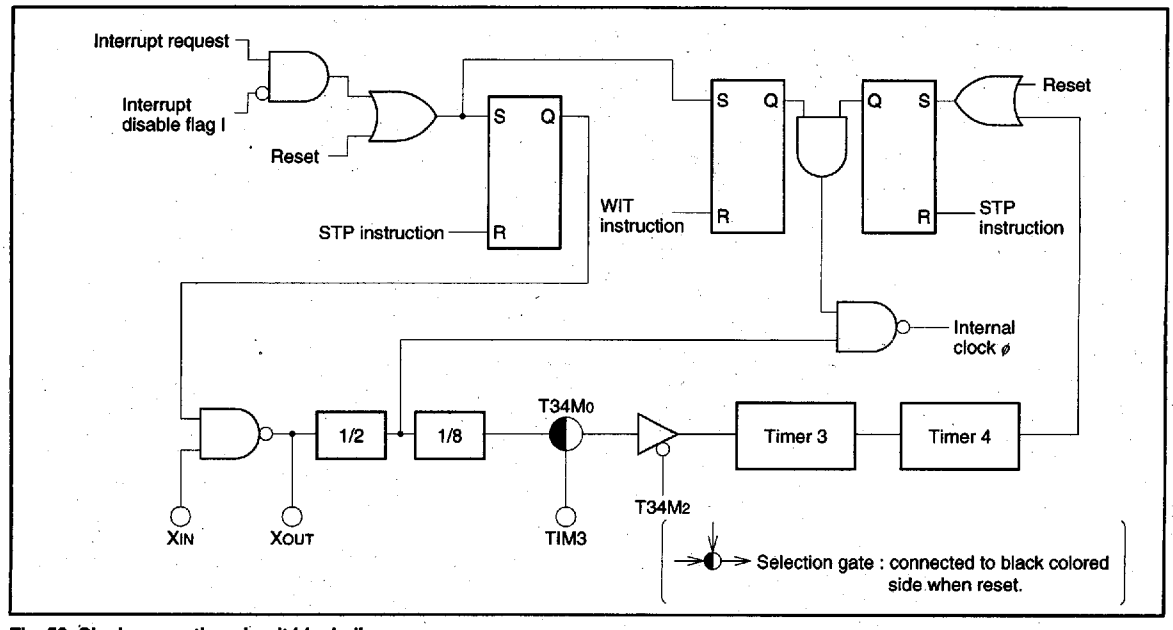


Fig. 50 Clock generating circuit block diagram

PROGRAMMING NOTES

(1) The divide ratio of the timer is 1/(n+1).
(2) Even though the BBC and BBS instructions are executed immediately after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. At least one instruction cycle is needed (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(3) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instruction is executed.
(4) An NOP instruction is needed immediately after the execution of a PLP instruction.
(5) In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{CC} pin and V_{SS} pin using a thick wire.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:
(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form (28-pin DIP Type 27256, three identical copies)

PROM Programming Method

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Product	Name of Programming Adapter
M37102E8SP	PCA4724
M37102E8FP	PCA4725
M37201E6SP	PCA4723
M37201E6FP	PCA4725

Note : In the case of M37102E6FP, after moving data of display ROM to addresses 3000_{16} to $3FFF_{16}$, write the data.

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 51 is recommended to verify programming.

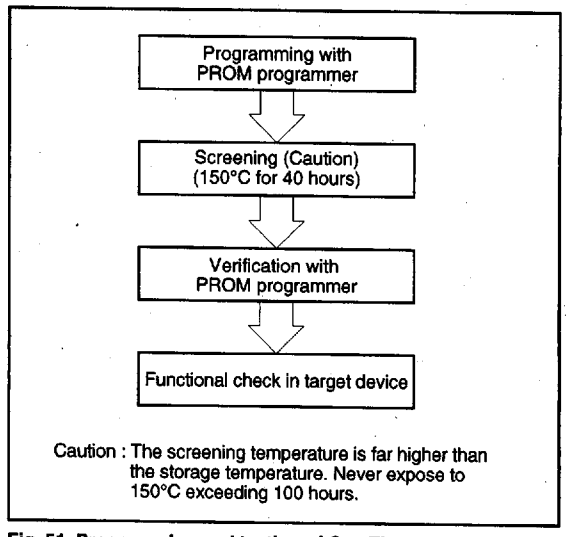


Fig. 51 Programming and testing of One Time PROM version

M37102M8-XXXSP/FP, M37102E8-XXXSP/FP, M37102E8SP/FP
M37201M6-XXXSP/FP, M37201E6-XXXSP/FP, M37201E6SP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	−0.3 to 6	V
V_I	Input voltage CNVss		−0.3 to 6	V
V_I	Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-03_6, $P4_0$-$P4_7$, $P6_0$-$P6_7$, H_{SYNC}, V_{SYNC}, $\overline{RESET}$		−0.3 to Vcc+0.3	V
V_O	Output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_6$, $P4_0$-$P4_5$, R, G, B, I, OUT, D-A, X_{OUT}, OSC2		−0.3 to Vcc+0.3	V
V_O	Output voltage $P4_6$, $P4_7$, $P6_0$-$P6_7$		−0.3 to 13	V
I_{OH}	Circuit current R, G, B, I, OUT, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$, $P3_1$, D-A		0 to 1 (Note 1)	mA
I_{OL1}	Circuit current R, G, B, I, OUT, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_6$, $P4_0$-$P4_3$, D-A		0 to 2 (Note 2)	mA
I_{OL2}	Circuit current $P6_0$-$P6_7$, $P4_6$, $P4_7$		0 to 1 (Note 2)	mA
I_{OL3}	Circuit voltage $P2_4$-$P2_7$		0 to 10 (Note 3)	mA
I_{OL4}	Circuit current $P4_4$, $P4_5$		0 to 3 (Note 2)	mA
P_d	Power dissipation	Ta=25°C	550	mW
T_{opr}	Operating temperature		−10 to 70	°C
T_{stg}	Storage temperature		−40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=−10 to 70°C unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Power source (Note 4) During the CPU and the CRT operation	4.5	5.0	5.5	V
V_{SS}	Power source	0	0	0	V
V_{IH}	"H" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_6$, $P4_0$-$P4_3$, $P4_6$, $P4_7$, $P6_0$-$P6_7$, H_{SYNC}, V_{SYNC}, $\overline{RESET}$, X_{IN}, OSC1	0.8Vcc		Vcc	V
V_{IH}	"H" input voltage $P4_4$, $P4_5$	0.7Vcc		Vcc	V
V_{IL}	"L" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P3_5$, $P4_0$, $P4_3$-$P4_5$, $P4_7$	0		0.4Vcc	V
V_{IL}	"L" input voltage TIM2, TIM3, INT1, S_{CLK1}, S_{IN1}, S_{IN2}, H_{SYNC}, V_{SYNC}, $\overline{RESET}$, X_{IN}, OSC1	0		0.2Vcc	V
I_{OH}	"H" average output current (Note 1) R, G, B, I, OUT, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$			1	mA
I_{OL1}	"L" average output current (Note 2) R, G, B, I, OUT, $P0_0$-$P0_7$, $P2_0$-$P2_3$, $P3_0$-$P3_6$, $P4_0$-$P4_3$, D-A			2	mA
I_{OL2}	"L" average output current (Note 2) $P6_0$-$P6_7$, $P4_6$, $P4_7$			1	mA
I_{OL3}	"L" average output current (Note 3) $P2_4$-$P2_7$			10	mA
I_{OL4}	"L" average output current (Note 2) $P4_4$, $P4_5$			3	mA
f_{CPU}	Oscillation frequency (for CRT operation) (Note 5)	3.6	4.0	4.4	MHz
f_{CRT}	Oscillation frequency (for CRT display)	6.0	7.0	8.0	MHz
f_{hs}	Input frequency TIM2, TIM3, INT1, INT2, S_{CLK2},			100	kHz
f_{hs}	Input frequency S_{CLK1}			1	MHz

Notes 1: The total current that flows out of the IC should be 20mA (max.).
2: The total of I_{OL1}, I_{OL2} and I_{OL4} should be 30mA (max.).
3: The total of I_{OL} of port $P2_4$-$P2_7$ should be 20mA (max.).
4: Connect 0.022μF or more capacitor externally between the V_{CC} – V_{SS} power source pins so as to reduce power source noise.
Also connect 0.068μF or more capacitor externally between the V_{CC} – CNVss pins.
5: Use a quartz-crystal oscillator or a ceramic resonator for CPU oscillation circuit.

M37102M8-XXXSP/FP, M37102E8-XXXSP/FP, M37102E8SP/FP
M37201M6-XXXSP/FP, M37201E6-XXXSP/FP, M37201E6SP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

ELECTRIC CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10 to 70°C, f(X_{IN})=4MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC}	Power source current	V_{CC}=5.5V, f(X_{IN})=4MHz CRT OFF		10	20	mA
		V_{CC}=5.5V, f(X_{IN})=4MHz CRT ON		20	30	
		At stop mode			300	μA
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, R, G, B, I, OUT	V_{CC}=4.5V I_{OH}=−0.5mA	2.4			V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_6$, $P4_0$-$P4_3$, B, G, B, I, OUT, D-A	V_{CC}=4.5V I_{OL}=0.5mA			0.4	V
	"L" output voltage $P6_0$-$P6_7$, $P4_6$, $P4_7$	V_{CC}=4.5V I_{OL}=0.5mA			0.4	
	"L" output voltage $P2_4$-$P2_7$	V_{CC}=4.5V I_{OL}=10mA			3.0	
	"L" output voltage $P4_4$, $P4_5$	V_{CC}=4.5V I_{OL}=3mA			0.4	
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC}=5.0V		0.5	0.7	V
	Hysteresis (Note) H_{SYNC}, V_{SYNC}, $P3_2$-$P3_4$, $P3_6$, $P4_1$, $P4_2$, $P4_4$-$P4_6$	V_{CC}=5.0V		0.5	1.3	
I_{OZH}	"H" input leak current $\overline{RESET}$, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_6$, $P4_0$-$P4_5$	V_{CC}=5.5V V_O=5.5V			5	μA
	"H" input leak current $P6_0$-$P6_7$, $P4_6$, $P4_7$	V_{CC}=5.5V V_O=12V			10	
I_{OZL}	"L" input leak current $\overline{RESET}$, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_6$, $P4_0$-$P4_7$, $P6_0$-$P6_7$	V_{CC}=5.5V V_O=0V			5	μA

Note : $P3_2$-$P3_4$, $P3_6$ have the hysteresis when these pins are used as interrupt input pins or timer input pins.
$P4_1$, $P4_2$, $P4_4$-$P4_6$ have the hysteresis when these pins are used as serial I/O ports.

Note 28. Self refresh sequence

Two refreshing ways should be used properly depending on the low pulse width (t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. In case of $t_{RASS} < 300ms$

1.1 Distriduted refresh during Read/Write operation

(A) Timing Diagrams

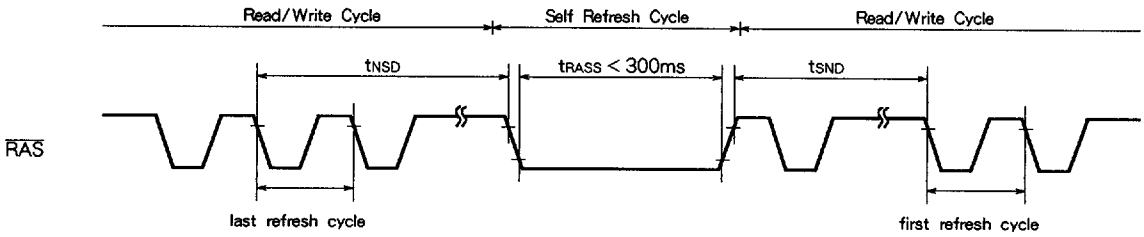


Table 2

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR distributed refresh	$t_{NSD} + t_{SND} \leqq 16.4ms$	
$\overline{RAS}$ only distributed refresh	$t_{NSD} \leqq 16\ \mu s$	$t_{SND} \leqq 16\ \mu s$

(B) Definition of refresh

Definition of CBR distributed refresh

The CBR distributed refresh performs more then 1024 discrete CBR cycles within 16.4 ms.

Definition of $\overline{RAS}$ only distributed refresh

All combination of ten row address signals (A_0~A_9) are selected during 1024 discrete $\overline{RAS}$ only refresh cycles within 16.4 ms.

1.1.1 CBR distributed Refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2).

1.1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs.

1.2 Burst refresh during Read/Write operation

(A) Timing diagram

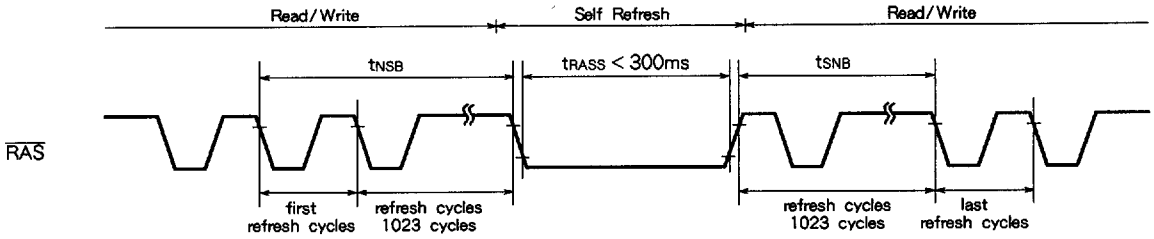


Table 3

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR burst refresh	$t_{NSB} \leqq 16.4ms$	$t_{SNB} \leqq 16.4ms$
RAS only burst refresh	$t_{NSB} + t_{SNB} \leqq 16.4ms$	

(B) Definition of burst refresh

Definition of CBR burst refresh

The CBR burst refresh performs more then 1024 continuous CBR cycles within 16.4ms.

Definition of RAS only burst refresh

All combination of ten row address signals (A_0~A_9) are selected during 1024 continuous RAS only refresh cycles within 16.4 ms.

1.2.1 CBR distributed Refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSB} from the falling edge of RAS signal in the first CBR refresh cycle during read/write operation period to the falling edge of RAS signal at the start of self refresh operation should be set within 16.4 ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SNB} from the rising edge of RAS signal at the end of self refresh operation to the falling edge of RAS signal in the last CBR refresh cycle during read /write operation period should be set within 16.4 ms.

1.2.2 RAS only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of RAS signal in the first RAS only refresh cycle during read/write operation period to the falling edge of RAS signal at the start of self refresh operation should be set within t_{NSB} (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of RAS signal at the end of self refresh operation to the falling edge of RAS signal in the last RAS only refresh cycle during read/ write operation period should be set within t_{SNB} (shown in table 3).

2. In case of $t_{RASS} \geqq 300ms$
(A) Timing diagram

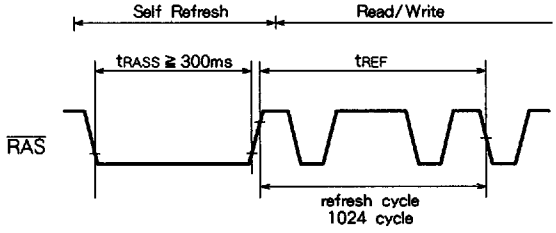


Table 4

Read/Write	Self Refresh→Read/Wirte
CBR distributed refresh $\overline{RAS}$ only distributed refresh CBR burst refresh $\overline{RAS}$ only burst refresh	$t_{REF} \leqq 16.4ms$

(B) Definition of refresh
The same as 1.1-(B) and 1.2-(B)

2.1
Regardless of the refresh (CBR distributed refresh, $\overline{RAS}$ only distributed refresh, CBR burst refresh, $\overline{RAS}$ only burst refresh) during Read/Write operation the minimum of 1024 cycles refresh should be preformed within 16.4 ms from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation.