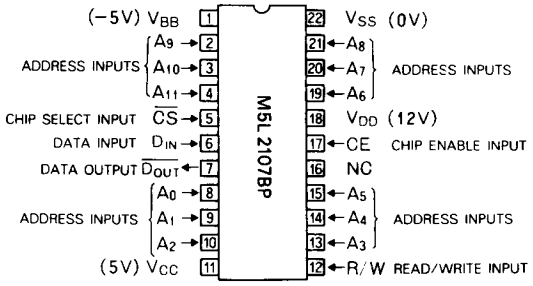
DESCRIPTION

These devices are 4096-word by 1-bit dynamic RAMs, fabricated with the N-channel silicon-gate MOS process. These RAMs are designed for large-capacity memory systems where high speed, low power dissipation and low cost are important design objects.

FEATURES

- Fast access time: 200ns (max)
- Fast cycle time: 400ns (min)
- Low active power: 300mW (typ)
- Low standby power: 0.03μW/bit (typ)
- Voltage range for all power supplies (V_{DD}, V_{CC}, V_{BB}): ±10%
- Refresh interval: 2ms (Ta = 0~70°C)
- Refresh addresses: A_0, A_1, A_2, A_3, A_4, A_5
- All inputs except CE terminal are directly TTL compatible
- Memory expansion is enabled by chip select input
- Output can be in the floating (high-impedance) state when $\overline{CS}$ is high or CE is low.
- Interchangeable with Intel's 2107B and TI's TMS4060

PIN CONFIGURATION (TOP VIEW)



NC = NO CONNECTION

Outline 22P1 (M5L 2107BP)
22S1 (M5L 2107BS)

APPLICATION

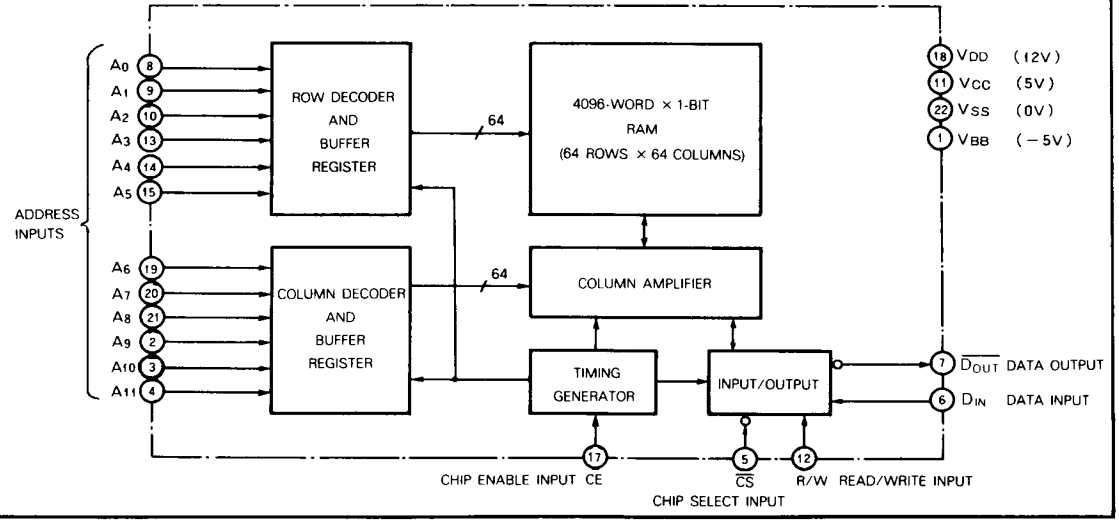
- Main memory unit for computers

FUNCTION

A location is designated by address signals A_0~A_{11}, and reading from and writing to that location is controlled by R/W. When $\overline{CS}$ is high, the chip is in the non-selectable state, disabling both read and write operations.

The devices are dynamic RAMs, and must be refreshed every 2ms to hold data stored in the memory cells. Refreshing is performed by reading sequentially the 64 locations designated by the 6 address signals A_0~A_5.

BLOCK DIAGRAM



4096-BIT (4096-WORD BY 1-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Limits	Unit
V_{DD}	Supply voltage		With respect to V_{BB} (substrate)	−0.3～20	V
V_{CC}	Supply voltage			−0.3～20	V
V_{SS}	Supply voltage			−0.3～20	V
V_I	Input voltage			−0.3～20	V
V_O	Output voltage			−0.3～20	V
P_d	Power dissipation	M5L 2107BP	Ta＝25℃	700	mW
		M5L 2107BS	Ta＝25℃	1000	mW
T_{opr}	Operating free-air temperature range			0～70	℃
T_{stg}	Storage temperature range	M5L 2107BP		−40～125	℃
		M5L 2107BS		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	10.8	12	13.2	V
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{BB}	Supply voltage	−4.5	−5	−5.5	V
$V_{IH(CE)}$	High-level chip enable input voltage	$V_{DD}-1$		$V_{DD}+1$	V
V_{IH}	High-level input voltage, all inputs except chip enable	2.4		$V_{CC}+1$	V
$V_{IL(CE)}$	Low-level chip enable input voltage	−1		1	V
V_{IL}	Low-level input voltage, all inputs except chip enable	−1		0.6	V

ELECTRICAL CHARACTERISTICS

(Ta＝0～70°C, V_{DD}＝12V±10%, V_{CC}＝5V±10%, V_{SS}＝0V, V_{BB}＝−5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{IH(CE)}$	High-level chip enable input voltage		$V_{DD}-1$		$V_{DD}+1$	V
V_{IH}	High-level input voltage, all inputs except chip enable		2.4		$V_{CC}+1$	V
$V_{IL(CE)}$	Low-level chip enable input voltage		−1		1	V
V_{IL}	Low-level input voltage, all inputs except chip enable		−1		0.6	V
$I_{I(CE)}$	Input current, chip enable input	$V_I=V_{DD}+1V$		0.01	2	μA
I_I	Input current, all inputs except chip enable	$V_I=6.5V$		0.01	10	μA
V_{OH}	High-level output voltage	$I_{OH}=-2mA$	2.4		V_{CC}	V
V_{OL}	Low-level output voltage	$I_{OL}=2mA$	0		0.45	V
I_{OZ}	Off-state output current	$V_{OZ}=0\sim V_{CC}$			±10	μA
I_{DD1}	Supply current from V_{DD}	$V_{IL(CE)}=-1V\sim 0.6V$		10	200	μA
I_{DD2}	Supply current from V_{DD}	$V_{IH(CE)}=V_{IH}$, $V_{IL}(\overline{CS})=V_{IL}$		10	25	mA
I_{CC}	Supply current from V_{CC}	$V_{IL(CE)}=V_{IL}$ or $V_{IH}(\overline{CS})=V_{IH}$		0.01	10	μA
I_{BB}	Supply current from V_{BB}			0.01	100	μA
$I_{DD(AV)}$	Average supply current from V_{DD}	$t_{w(CE)}$＝230ns, t_C＝400ns		25	40	mA
$C_{I(CE)}$	Input capacitance, chip enable input	$V_{IL}=V_{SS}$, $V_{BB}=-5V$, f＝1MHz		17	25	pF
C_I	Input capacitance, all inputs except chip enable	$V_{IL}=V_{SS}$, $V_{BB}=-5V$, f＝1MHz		5	7	pF
C_O	Output capacitance	$V_{OL}=V_{SS}$, $V_{BB}=-5V$, f＝1MHz		5	7	pF

Note 1 : Current flowing into an IC is positive; out is negative.

TIMING REQUIREMENTS ($Ta=0\sim70°C$, $V_{DD}=12V\pm10\%$, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$, $V_{BB}=-5V\pm10\%$, unless otherwise noted)

Read, Write or Read-Modify-Write Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(REF)}$	Refresh cycle time				2	ms
$t_{w(\overline{CEL})}$	Chip enable low pulse width		130			ns
$t_{r(CE)}$	Chip enable pulse rise time				40	ns
$t_{f(CE)}$	Chip enable pulse fall time				40	ns
$t_{su(AD)}$	Address setup time		0			ns
$t_{su(\overline{CS})}$	Chip select setup time		0			ns
$t_{h(AD)}$	Address hold time		100			ns
$t_{h(\overline{CS})}$	Chip select hold time		100			ns

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Read Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(RD)}$	Read cycle time	$t_r=t_f=20ns$	400			ns
$t_{w(CEH)}$	Chip enable high pulse width		230		4000	ns
$t_{su(RD)}$	Read setup time		−10			ns
$t_{h(RD)}$	Read hold time		0			ns

Write or Read-Modify-Write Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(WR)}$	Write cycle time	$t_r=t_f=20ns$	400			ns
$t_{c(RMW)}$	Read-modify-write cycle time		520			ns
$t_{w(CEH)}$	Chip enable high pulse width.write cycle		230		4000	ns
$t_{w(CEH)}$	Chip enable high pulse width, read-modify-write cycle		350		4000	ns
$t_{su(RD)}$	Read setup time		−10			ns
$t_{h(RD)}$	Read hold time		180			ns
$t_{su(WR)}$	Write setup time		150			ns
$t_{w(WR)}$	Write pulse width		50			ns
$t_{d(WR)}$	Write delay time		150			ns
$t_{su(DA)}$	Data setup time		0			ns
$t_{h(DA)}$	Data hold time		0			ns

SWITCHING CHARACTERISTICS ($Ta=0\sim70°C$, $V_{DD}=12V\pm10\%$, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$, $V_{BB}=-5V\pm10\%$, unless otherwise noted)

Read Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(CE)}$	Chip enable access time	$C_L=50pF$, Load=1 TTL, $V_{REF}=2.0V$			180	ns
$t_{a(AD)}$	Address access time	$t_{su(AD)}=0ns$, $t_r=t_f=20ns$			200	ns
$t_{dv(CE)}$	Data valid time with respect to chip enable		0			ns

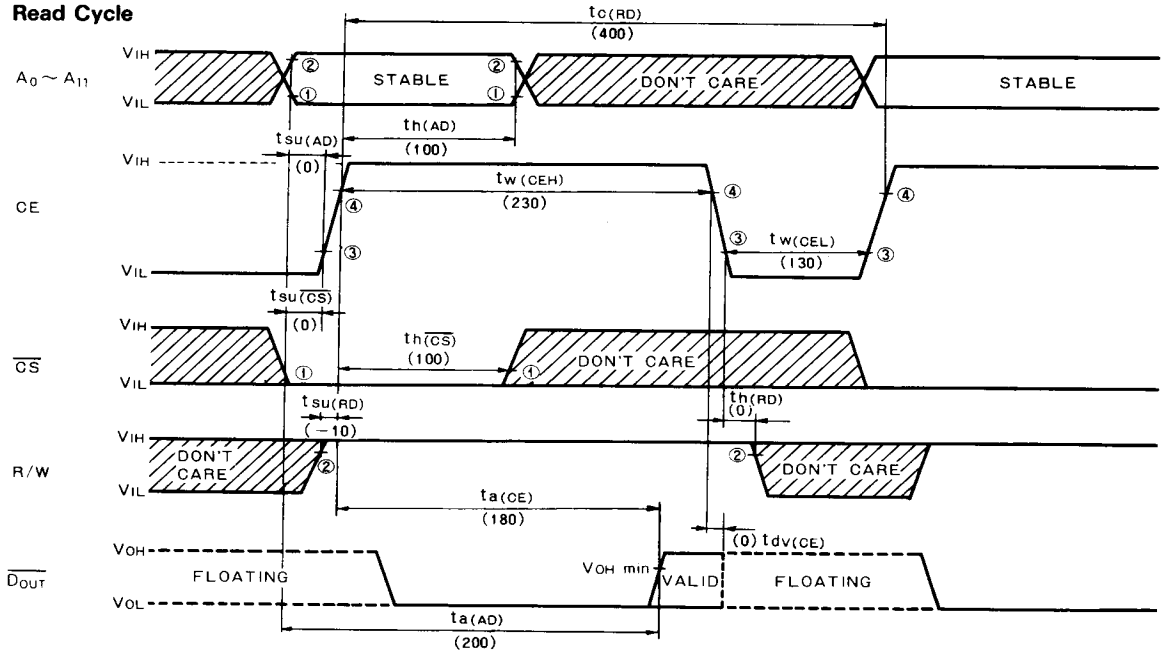
Read-Modify-Write Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(CE)}$	Chip enable access time	$C_L=50pF$, Load=1 TTL, $V_{REF}=2.0V$			180	ns
$t_{a(AD)}$	Address access time	$t_{su(AD)}=0ns$, $t_r=t_f=20ns$			200	ns
$t_{dv(CE)}$	Data valid time with respect to chip enable		0			ns

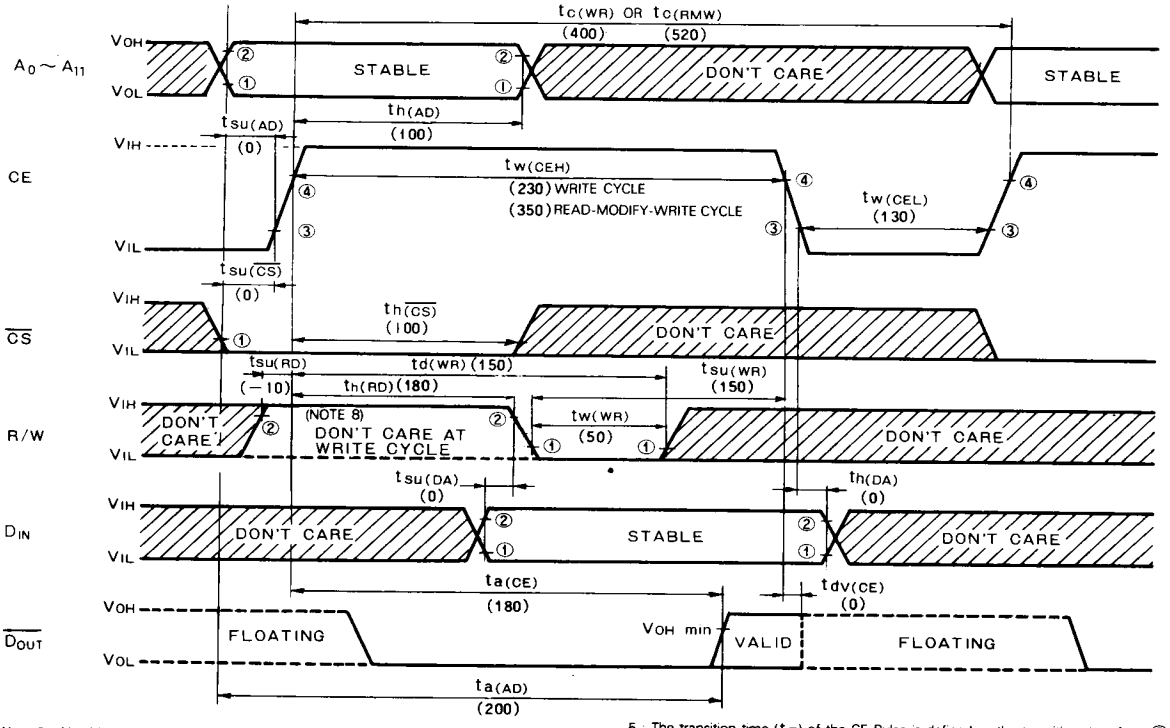
4096-BIT (4096-WORD BY 1-BIT) DYNAMIC RAM

TIMING DIAGRAMS

Read Cycle



Write or Read-Modify-Write Cycle



Note 2 : Hatching indicates the state is unknown or changing.

3 : Vss+0.8V is the reference level for point ①, and Vss+2.4V for point ②.

4 : Vss+2.0V is the reference level for point ③, and V_{DD} −2.0V for point ④.

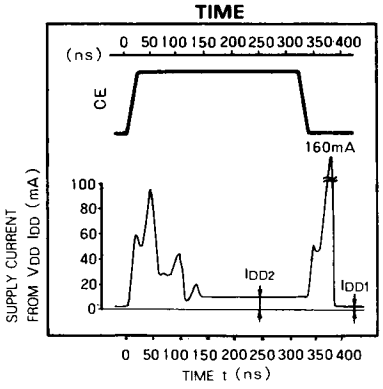
5 : The transition time (t_T) of the CE Pulse is defined as the transition time from ③ to ④ and from ④ to ③.

6 : The level of the dotted line should be kept high during read-modify-write cycle.

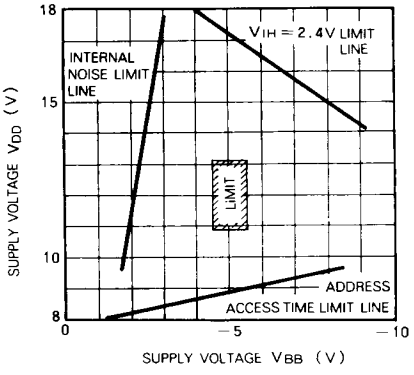
7 : Numbers in parentheses ( ) indicate the minimum timing value in ns.

TYPICAL CHARACTERISTICS

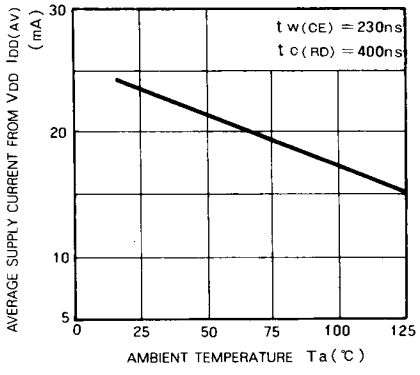
SUPPLY CURRENT FROM VDD VS. TIME



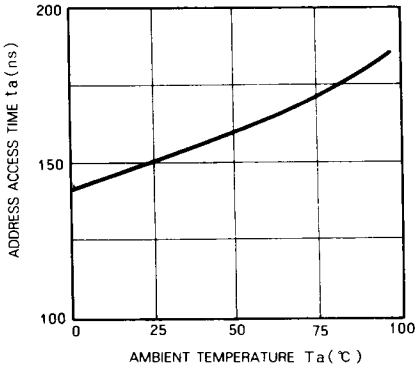
VDD VS. VBB OPERATING REGION



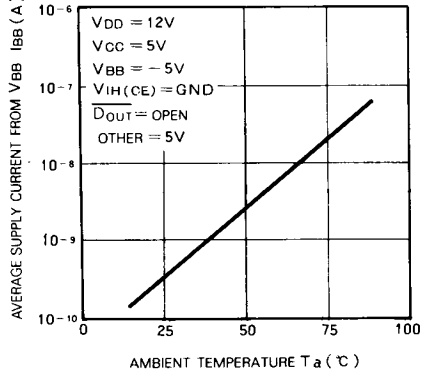
AVERAGE SUPPLY CURRENT FROM VDD VS. AMBIENT TEMPERATURE



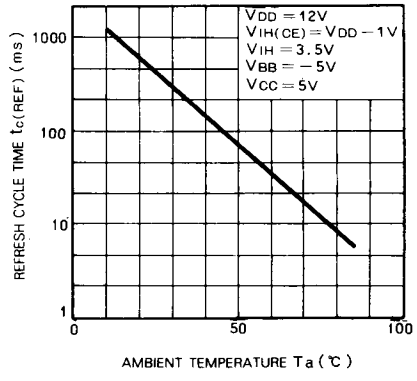
ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE



AVERAGE SUPPLY CURRENT FROM VBB VS. AMBIENT TEMPERATURE



REFRESH CYCLE TIME VS. AMBIENT TEMPERATURE



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4096-BIT (4096-WORD BY 1-BIT) DYNAMIC RAM

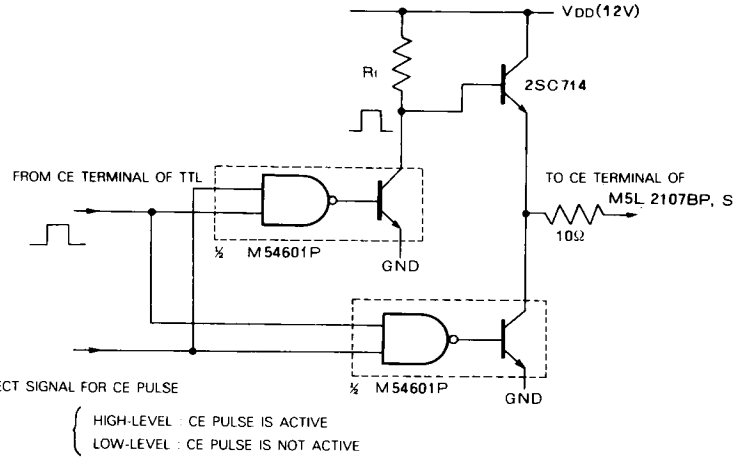
APPLICATION

Method of Refreshing

Since 64 memory cells designated by the X address can be refreshed in 1 cycle, (either read, write or read-modify-write), a read operation for all 64 addresses selected by the 6 address signals A_0~A_5 must be performed within 2ms to refresh all 4096 memory cells. If the chip is refreshed during a write cycle or a read-modify-write cycle, then signal $\overline{CS}$ must be kept low; during a read cycle, $\overline{CS}$ can be either high or low. If a read operation is executed when the chip is in the non-designated state with $\overline{CS}$ high, refreshing can be performed with the output terminal $\overline{D_{OUT}}$ in the floating (high-impedance) state. Thus all the M5L 2107BP, S used in the memory system can be refreshed in only 64 cycles.

Recommended Driver Circuit for Chip Enable Pulse

COMPONENTS : M54601P · · · · · · · 1
2SC714 · · · · · · · · · 1
RESISTORS · · · · · 2



Note 1 : R_1 is determined according to a required rise time of the CE pulse. For example, when C_L capacitance load for the CE pulse is 300pF.

R_1 is set at 300Ω ($\frac{1}{2}$W) ; then, rise time t_r = 30ns, fall time t_f = 30ns, t_{PHL} = 20ns, t_{PLH} = 20ns.

2 : One M54601P dual peripheral positive AND driver circuit should be used for each CE driver circuit