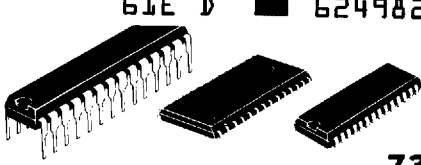


M5M5179AP, J, FP-15, -20, -25



73728-BIT(8192-WORD BY 9-BIT)CMOS STATIC RAM

MITSUBISHI (MEMORY/ASIC)

DESCRIPTION

This is a family of 8192 word by 9-bit static RAMs, fabricated with the high performance CMOS silicon gate MOS process and designed for high-speed application. 9 bit organization is useful for parity check system. These devices operate on a single 5V supply, and are directly TTL compatible.

FEATURES

- Fast access time
 - M5M5179AP, J, FP 15 ns (max.)
 - M5M5179AP, J, FP 20 ns (max.)
 - M5M5179AP, J, FP 25 ns (max.)
- 9 bit organization
- Single +5V Power Supply
- Fully Static Operation: No Clocks, No Refresh
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability
- Simple Memory Expansion by \overline{S}_1, S_2
- \overline{OE} Prevents Data Contention in The I/O Bus
- Common Data I/O

APPLICATION

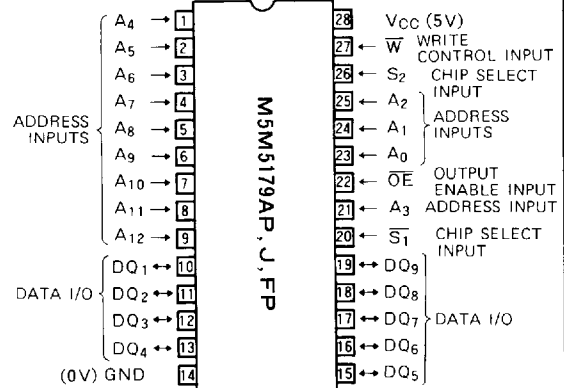
High-speed memory system

FUNCTION

The operation mode of the M5M5179A is determined by a combination of the device control inputs $\overline{S}_1, S_2, \overline{W}$ and \overline{OE} . Each mode is summarized in the function table. (see next page)

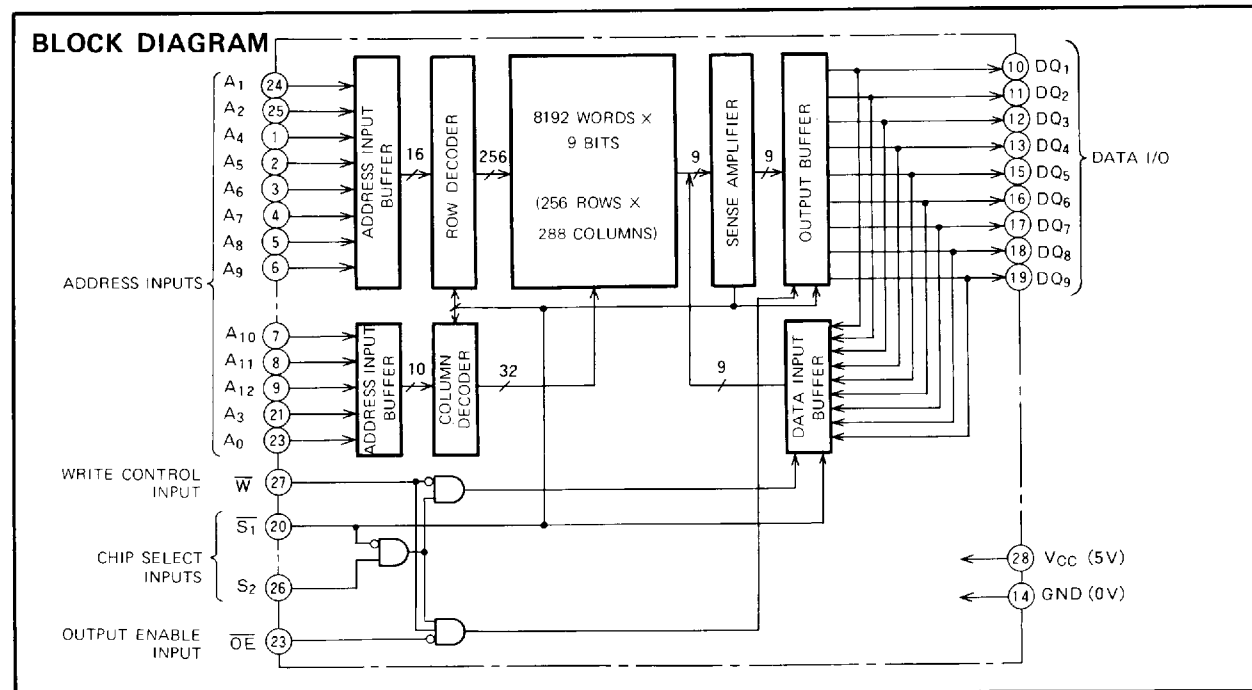
A write cycle is executed whenever the low level \overline{W} overlaps with the low level \overline{S}_1 and the high level S_2 . The

PIN CONFIGURATION (TOP VIEW)



28P4Y (P)
Outline 28P2W (FP)
28P0J (J)

address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}, \overline{S}_1$ or S_2 , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input \overline{OE} directly controls the output stage. Setting the \overline{OE} at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.



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A read cycle is executed by setting \overline{W} at a high level and \overline{OE} at a low level while $\overline{S_1}$ and S_2 are in an active state ($\overline{S_1} = L, S_2 = H$)

When setting $\overline{S_1}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S_1}$. The power supply current is reduced as low as the stand-by current which is specified at I_{CC2} or I_{CC3} .

FUNCTION TABLE

$\overline{S_1}$	S_2	\overline{W}	\overline{OE}	Mode	DO	I_{CC}
L	L	X	X	Non selection	high-impedance	Active
H	X	X	X	Non selection	high-impedance	Standby
L	H	L	X	Write	D_{IN}	Active
L	H	H	L	Read	D_{OUT}	Active
L	H	H	H		high-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	-0.3~7	V
V_I	Input voltage		-0.3~ $V_{CC}+0.3$	V
V_O	Output voltage		0~ V_{CC}	V
P_d	Power dissipation	$T_a=25^\circ C$	1000	mW
T_{opr}	Operating temperature		-10~85	$^\circ C$
T_{stg}	Storage temperature		-65~150	$^\circ C$

DC ELECTRICAL CHARACTERISTICS ($T_a=0\sim 70^\circ C$, $V_{CC}=5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IL}	Low input voltage		-0.3		0.6	V
V_{IH}	High input voltage		2.4		$V_{CC}+0.3$	V
V_{OH}	High output voltage	$I_{OH} = -4mA$	2.4			V
V_{OL}	Low output voltage	$I_{OL} = 8mA$			0.4	V
I_I	Input current	$V_I = 0 \sim V_{CC}$			± 1	μA
I_{OZH}	High level output current in off-state	$\overline{S_1} = V_{IH}$ or $S_2 = V_{IL}$ or $\overline{OE} = V_{IH}$			1	μA
I_{OZL}	Low level output current in off-state	$V_{I/O} = 0 \sim V_{CC}$			-1	μA
I_{CC1}	Active supply current	$\overline{S_1} = V_{IL}$ Output open Other inputs = V_{IH}	AC (25MHz)		120	mA
			DC		70	
I_{CC2}	Stand by supply current	$S_2 = V_{IL}, \overline{S_1} = V_{IH}$ Other inputs = $0 \sim V_{CC}$	AC (25MHz)		30	mA
			DC		20	
I_{CC3}	Stand by supply current	$\overline{S_1} \geq V_{CC} - 0.2V$ Other inputs $\leq 0.2V$ or $V_{CC} - 0.2V$			2	mA
C_i	Input capacitance	$\overline{S_1}, S_2, \overline{OE}, \overline{W}$	$V_I = GND, V_I = 25mV_{rms}, f = 1MHz$		7	μF
		$A_0 \sim A_{12}$			6	
C_o	Output capacitance	$V_O = GND, V_O = 25mV_{rms}, f = 1MHz$			8	μF

Note 1. Direction for current flowing into IC is indicated as positive (no mark)
 2. Typical value is $V_{CC} = 5V, T_a = 25^\circ C$.

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SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits									Unit
		M5M5179A-15			M5M5179A-20			M5M5179A-25			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{OR}	Read cycle time	15			20			25			ns
$t_{a(A)}$	Address access time			15			20			25	ns
$t_{s(S1)}$	Chip select 1 access time			15			20			25	ns
$t_{a(S2)}$	Chip select 2 access time			12			17			22	ns
$t_{a(OE)}$	Output enable access time			8			10			12	ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high			8			10			15	ns
$t_{dis(S2)}$	Output disable time after S_2 low			8			10			15	ns
$t_{dis(OE)}$	Output disable time after \overline{OE} high			8			10			15	ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	3			3			3			ns
$t_{en(S2)}$	Output enable time after S_2 high	2			2			2			ns
$t_{en(OE)}$	Output enable time after \overline{OE} low	2			2			2			ns
$t_{v(A)}$	Data valid time after address change	3			3			3			ns

TIMING REQUIREMENTS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Write cycle

Symbol	Parameter	Limits									Unit
		M5M5179A-15			M5M5179A-20			M5M5179A-25			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	15			20			25			ns
$t_{w(W)}$	Write pulse width	12			15			18			ns
$t_{su(A)}$	Address set up time	0			0			0			ns
$t_{su(S1)}$	Chip select 1 set up time	12			16			20			ns
$t_{su(S2)}$	Chip select 2 set up time	9			12			15			ns
$t_{su(D)}$	Data set up time	8			10			12			ns
$t_{h(D)}$	Data hold time	0			0			0			ns
$t_{rec(W)}$	Write recovery time	3			3			3			ns
$t_{dis(W)}$	Output disable time after \overline{W} low			8			10			12	ns
$t_{dis(OE)}$	Output disable time after \overline{OE} high			8			10			15	ns
$t_{en(W)}$	Output enable time after \overline{W} high	0			0			0			ns
$t_{en(OE)}$	Output enable time after \overline{OE} low	3			3			3			ns

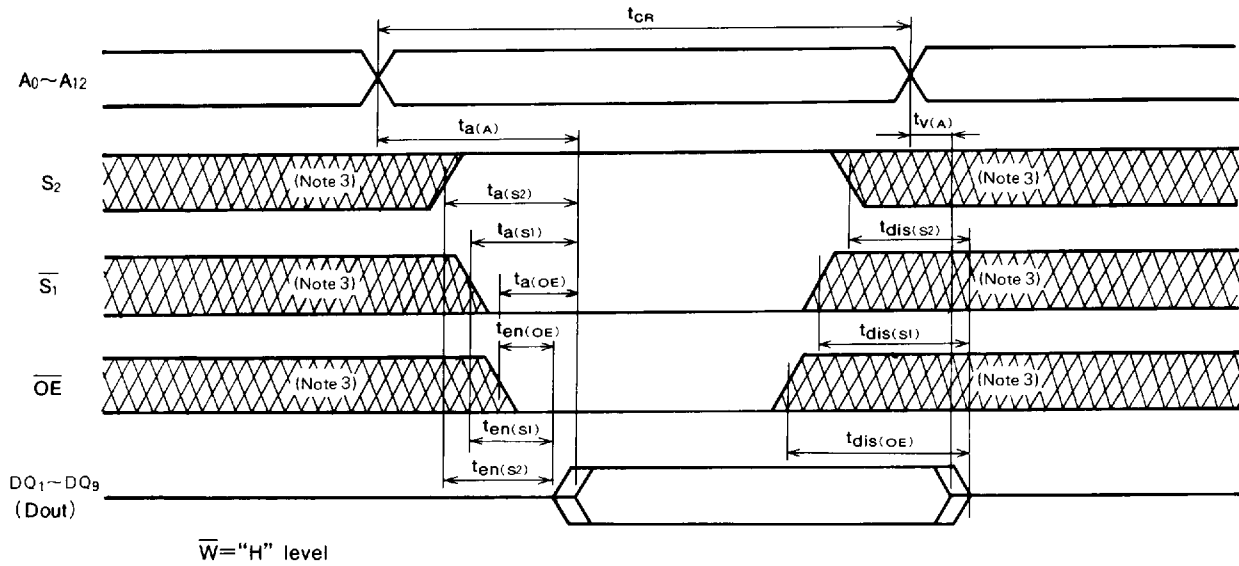
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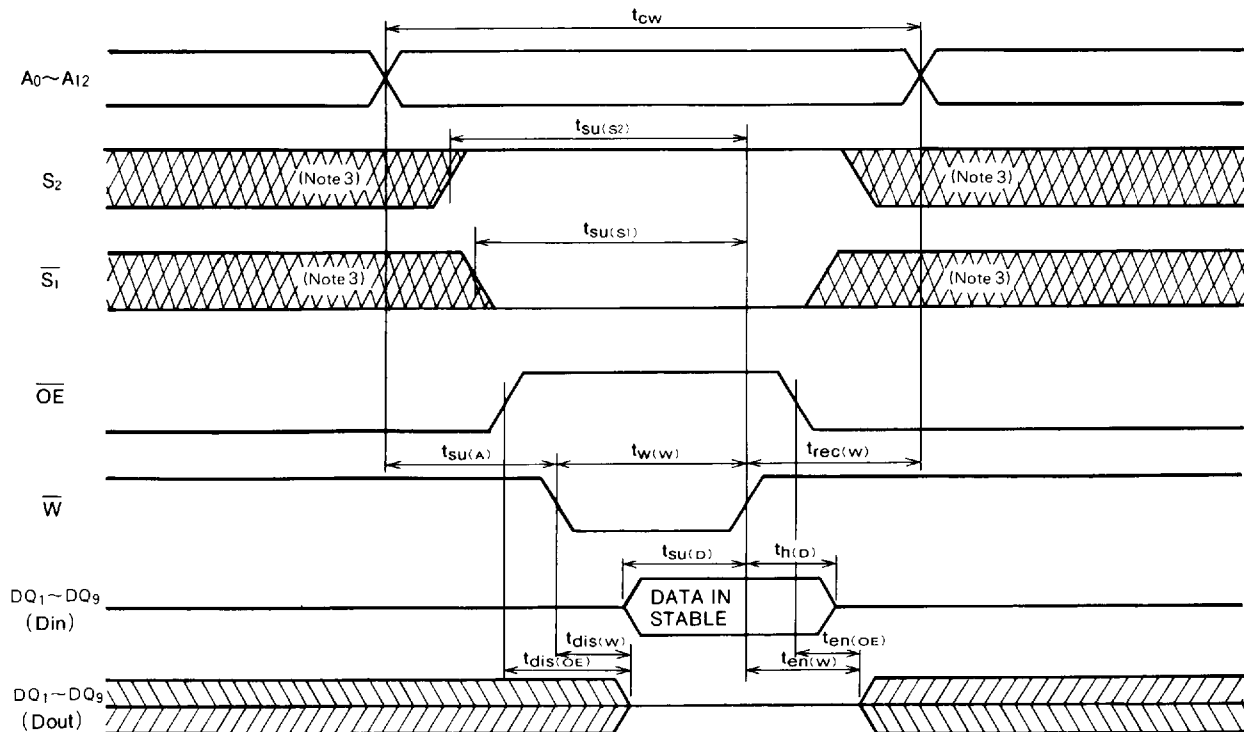
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TIMING DIAGRAM

Read cycle



Write cycle (\bar{W} control)

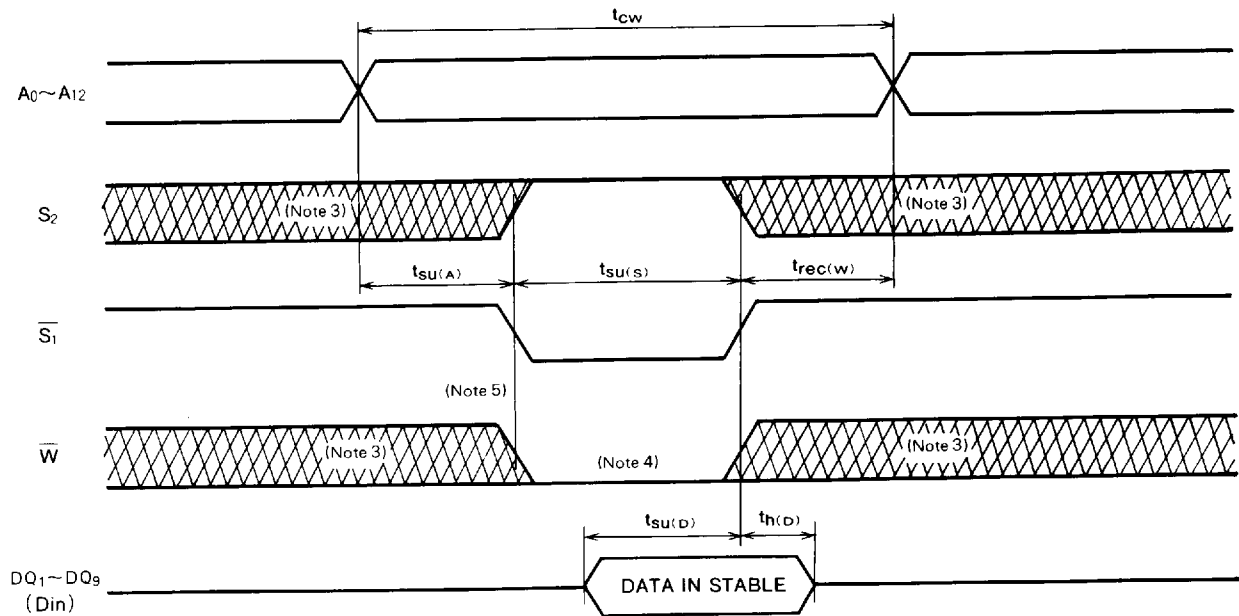


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Write cycle (\bar{S} control)



CONDITIONS

- Input pulse level $V_{IH} = 3V, V_{IL} = 0V$
- Input rise and fall time 3 ns
- Input timing standard level $V_{IH} = V_{IL} = 1.5V$
- Output timing reference level $V_{OH} = V_{OL} = 1.5V$
- Output loads Fig. 1, Fig. 2

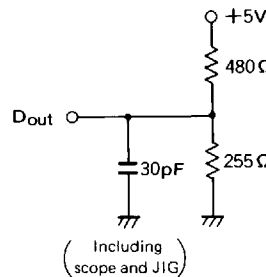


Fig. 1 Output load

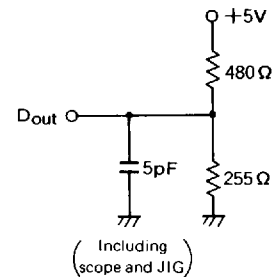


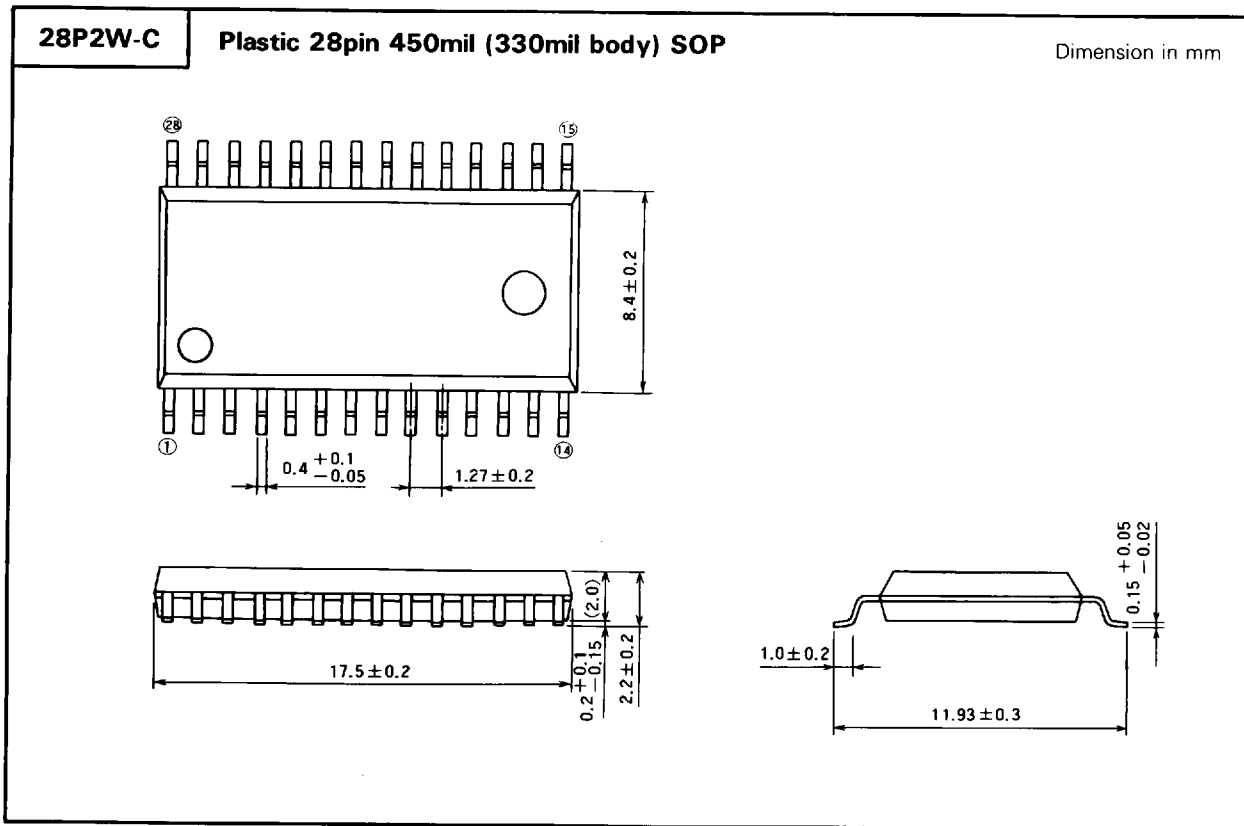
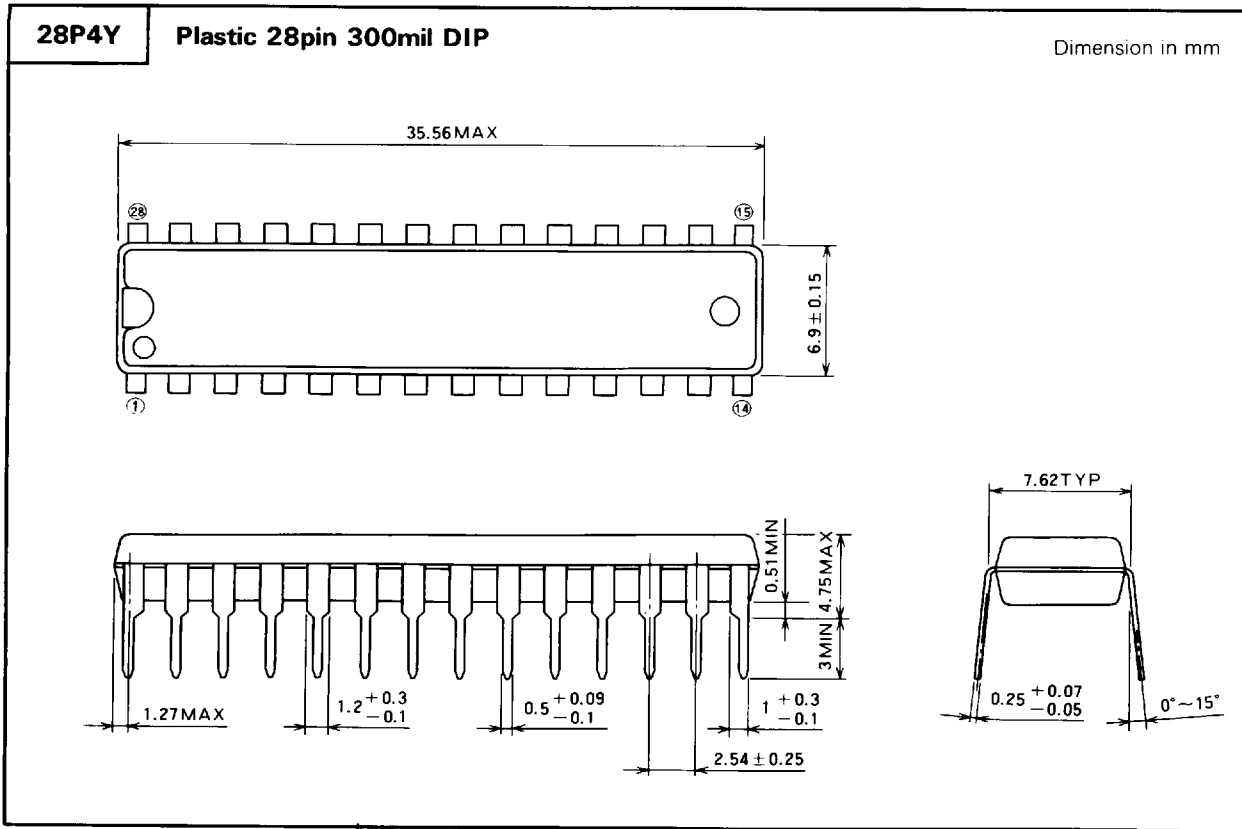
Fig. 2 Output load for $t_{en} t_{dis}$

- Note 3: Hatching indicates the state is don't care.
- 4: Writing is executed while S_2 high overlaps \bar{S}_1 and \bar{W} low.
- 5: If \bar{W} goes low simultaneously with or prior to \bar{S}_1 low or S_2 high, the output remains in the high-impedance state.
- 6: Don't apply inverted phase signal externally when DQ pin is in output mode.

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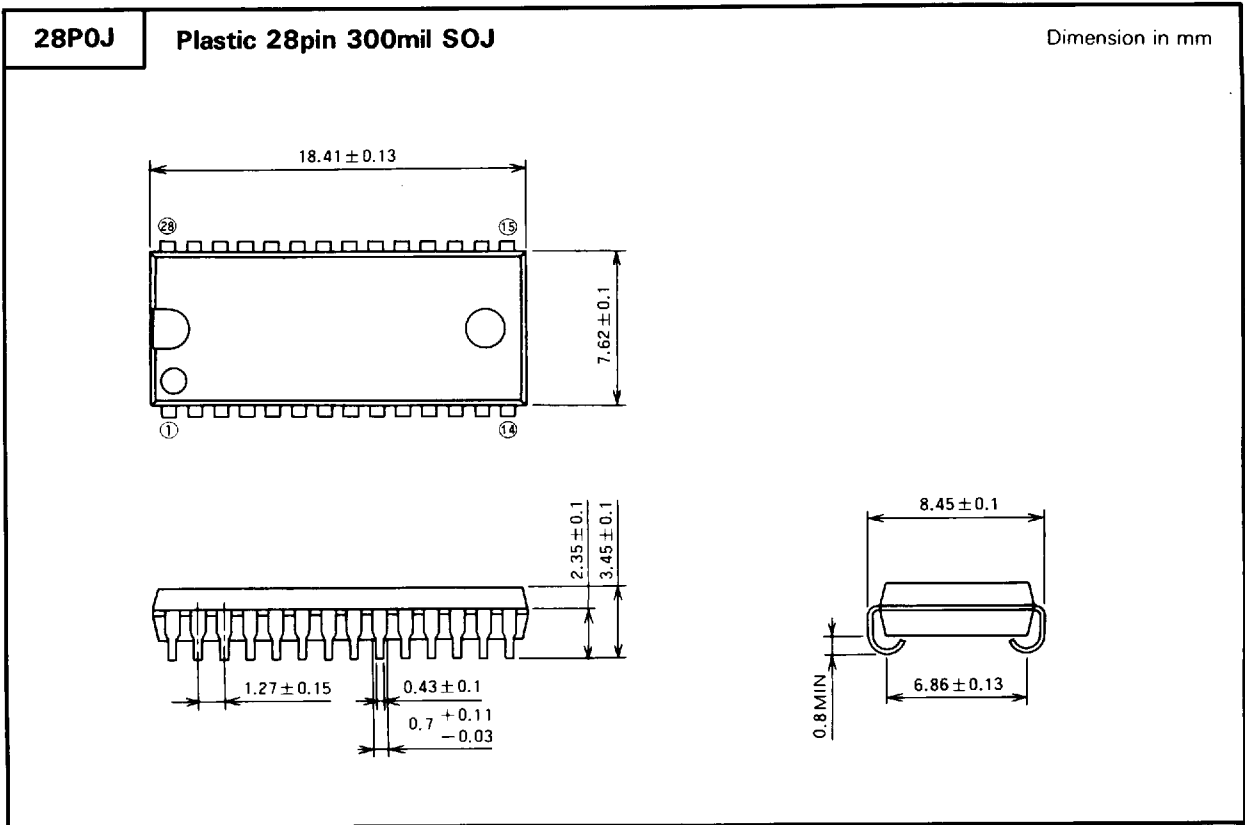
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