OBJECTIVE SPECIFICATION

2690-2—F,I,N • 2690-3—F,I,N • 2690-4—F,I,N

DESCRIPTION

The 2690 is fabricated with double-poly n-channel silicon gate technology for high performance and high functional density. It uses a single transistor dynamic storage cell and dynamic circuitry to achieve high speed and low power dissipation.

The unique design of the 2690 allows it to be packaged in the industry standard 16-pin in-line package, which provides the highest system bit densities and is compatible with widely available automated handling equipment.

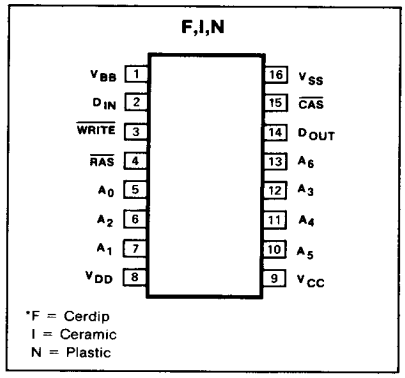
The use of the 16-pin package is made possible by multiplexing the 14 address bits (required to address one of 16,384 bits) into the 2690 on 7 address input pins. The two 7-bit address words are latched into the device by the 2 TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

The memory cell requires refreshing for data retention. This is most easily accomplished by performing a $\overline{RAS}$ only cycle at each of 128 row addresses every 2ms.

FEATURES

- **Access time:**
  - **2690-2: 150ns**
  - **2690-3: 200ns**
  - **2690-4: 250ns**
- **Read and write cycle time:**
  - **2690-2: 375ns**
  - **2690-3: 375ns**
  - **2690-4: 410ns**
- **Low power:**
  - **Operating: 462mW (max)**
  - **Standby: 20mW (max)**
- **±10% power supply margins**
- **On-chip latches for address and data in**
- **Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow 2-dimensional chip selection and extended page boundary**
- **Page mode addressing**
- **$\overline{RAS}$ only refresh**
- **Common I/O capability using "early write" operation**
- **All inputs TTL compatible**
- **3-state TTL compatible output**

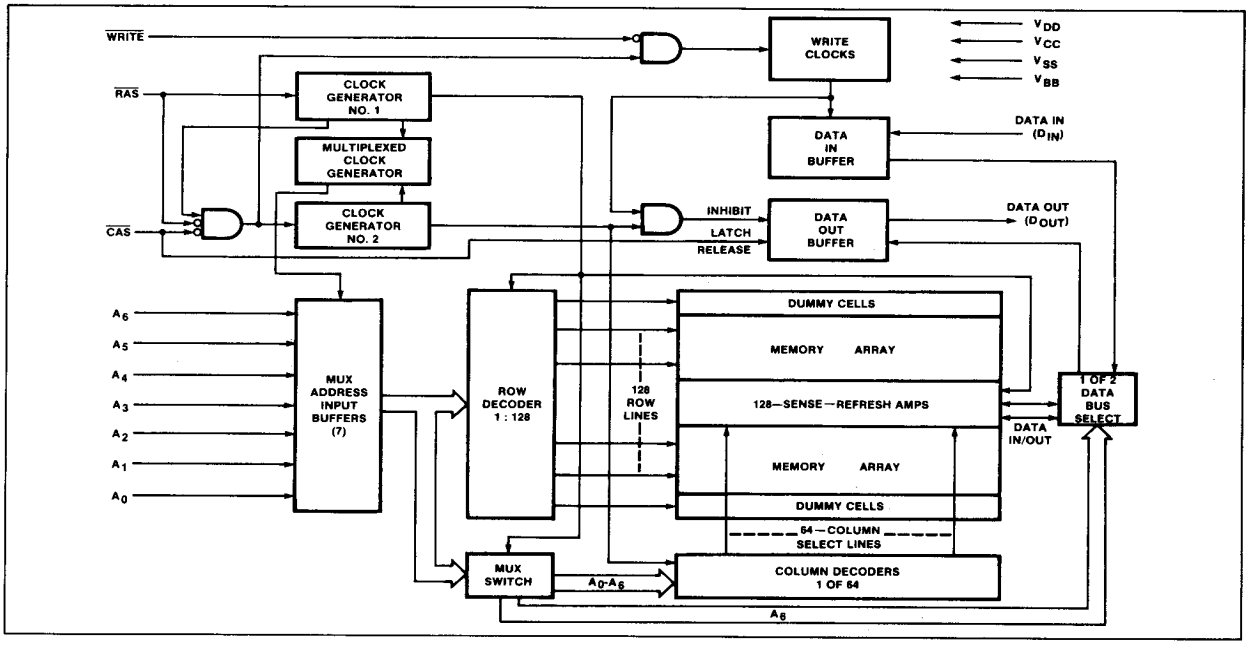
PIN CONFIGURATION



PIN DESIGNATION

PIN NO.	SYMBOL	NAME & FUNCTION
5-7, 10-13	A_0-A_6	Address inputs
15	$\overline{CAS}$	Column address strobe
2	D_{IN}	Data in
14	D_{OUT}	Data out
4	$\overline{RAS}$	Row address strobe
3	$\overline{WRITE}$	Read/write input
1	V_{BB}	Power (-5V)
9	V_{CC}	Power (+5V)
8	V_{DD}	Power (+12V)
16	V_{SS}	Ground

BLOCK DIAGRAM



MOS MEMORY

AC CHARACTERISTICS[7,8,9]

T_A = 0°C to +70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V unless otherwise specified.

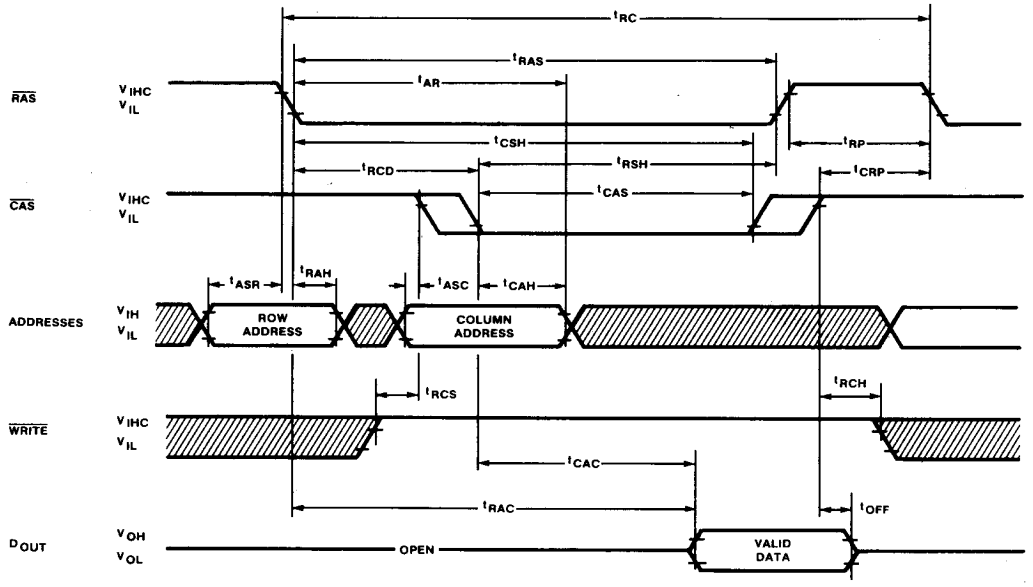
SYMBOL	PARAMETER	TEST CONDITIONS	2690-2		2690-3		2690-4		UNIT
			Min	Max	Min	Max	Min	Max	
	READ OR WRITE (EARLY) CYCLE								
t_{REF}	Refresh			2		2		2	ms
t_T[9]	Transition		3	35	3	50	3	50	ns
t_{RC}[15]	Random cycle		320		375		410		ns
t_{RAS}	$\overline{RAS}$ duration		150	10000	200	10000	250	10000	ns
t_{RP}	$\overline{RAS}$ precharge		100		120		150		ns
t_{RCD}[10]	Strobe delay		20	50	25	65	35	85	ns
t_{CAS}	$\overline{CAS}$ duration		100	10000	135	10000	165	10000	ns
t_{CRP}	$\overline{CAS}$ precharge		−20		−20		−20		ns
t_{RSH}	$\overline{RAS}$ hold		100		135		165		ns
t_{CSH}	$\overline{CAS}$ hold		150		200		250		ns
t_{ASR}	Row address set up		0		0		0		ns
t_{RAH}	Row address hold		20		25		35		ns
t_{ASC}	Column address set up		−10		−10		−10		ns
t_{CAH}	Column address hold		45		55		75		ns
t_{AR}	Address hold		95		120		160		ns
	READ CYCLE								
t_{RCS}	Read set up		0		0		0		ns
t_{RCH}	Read hold		0		0		0		ns
t_{OFF}[14]	Output turn off delay		0	40	0	50	0	60	ns
t_{RAC}[12,13]	Row access			150		200		250	ns
t_{CAC}[11,12]	Column access			100		135		165	ns
	WRITE (EARLY) CYCLE								
t_{WCS}[17]	Write set up		−20		−20		−20		ns
t_{WCH}	Write hold		45		55		75		ns
t_{WP}	Write duration		45		55		75		ns
t_{RWL}	Write to $\overline{RAS}$ lead		50		70		85		ns
t_{CWL}	Write to $\overline{CAS}$ lead		50		70		85		ns
t_{WCR}	Write to $\overline{RAS}$ hold		95		120		160		ns
t_{DS}[16]	Data set up		0		0		0		ns
t_{DH}[16]	Data hold		45		55		75		ns
t_{DHR}	Data to $\overline{RAS}$ hold		95		120		160		ns

NOTES

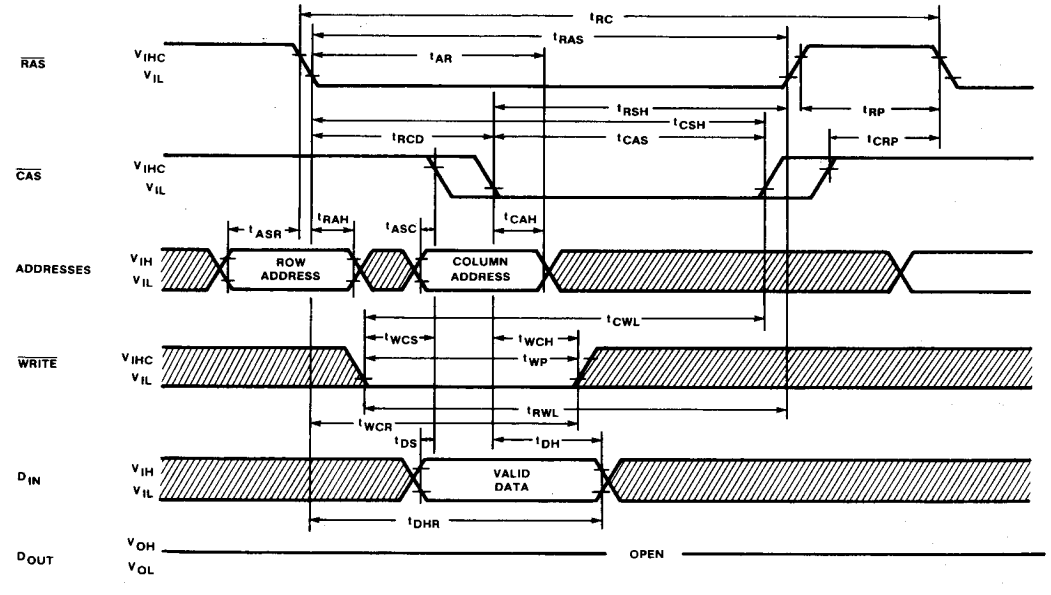
7. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
8. Ac measurements assume t_T = 5ns.
9. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
10. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
12. Measured with a load equivalent to 2 TTL loads and 100pF.
13. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value specified, t_{RAC} will increase by the amount that t_{RCD} exceeds the value specified.
14. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
15. The specifications for t_{RMW} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
16. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read/modify/write cycles.
17. t_{WCS} t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read/write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE (EARLY WRITE)



MOS MEMORY

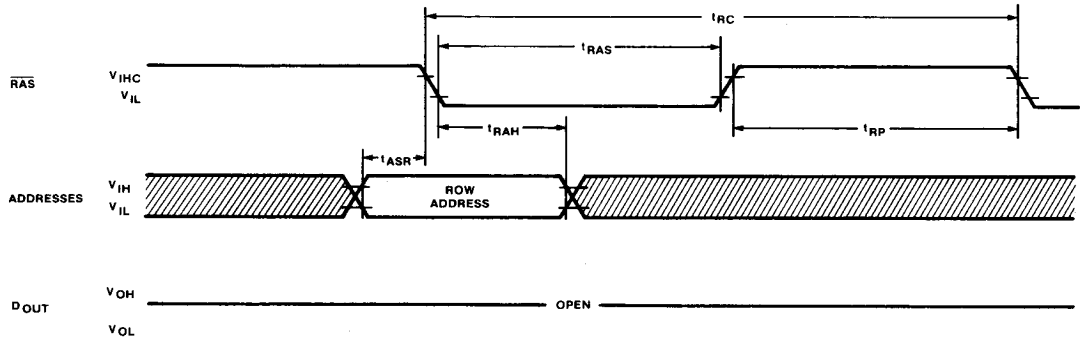
AC CHARACTERISTICS[7,8,9]

T_A = 0°C to +70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	2690-2		2690-3		2690-4		UNIT
			Min	Max	Min	Max	Min	Max	
	$\overline{RAS}$ ONLY REFRESH CYCLE								
t_{REF}	Refresh			2		2		2	ms
t_T[9]	Transition		3	35	3	50	3	50	ns
t_{RC}[15]	Random cycle		320		375		410		ns
t_{RAS}	$\overline{RAS}$ duration		150	10000	200	10000	250	10000	ns
t_{RP}	$\overline{RAS}$ precharge		100		120		150		ns
t_{ASR}	Row address set up		0		0		0		ns
t_{RAH}	Row address hold		20		25		35		ns
	READ/WRITE OR READ/MODIFY/WRITE								
t_{REF}	Refresh			2		2		2	ms
t_T[9]	Transition		3	35	3	50	3	50	ns
t_{RWC}	Read/write cycle		320		375		515		ns
t_{RMW}	Read/modify/write cycle		320		405		515		ns
t_{RRAS}	R/W $\overline{RAS}$ duration		185	10000	245	10000	305	10000	ns
t_{MRAS}	RMW $\overline{RAS}$ duration		215	10000	285	10000	355	10000	ns
t_{RP}	$\overline{RAS}$ precharge		100		120		150		ns
t_{RCD}[10]	Strobe delay		20	50	25	65	35	85	ns
t_{RCAS}	R/W $\overline{CAS}$ duration		135	10000	180	10000	230	10000	ns
t_{MCAS}	RMW $\overline{CAS}$ duration		165	10000	220	10000	270	10000	ns
t_{CRP}	$\overline{CAS}$ precharge		−20		−20		−20		ns
t_{RSH}	$\overline{RAS}$ hold		100		135		165		ns
t_{CSH}	$\overline{CAS}$ hold		150		200		250		ns
t_{ASR}	Row address set up		0		0		0		ns
t_{RAH}	Row address hold		20		25		35		ns
t_{ASC}	Column address set up		−10		−10		−10		ns
t_{CAH}	Column address hold		45		55		75		ns
t_{AR}	Address hold		95		120		160		ns
t_{RCS}	Read set up		0		0		0		ns
t_{RWD}	$\overline{RAS}$ to write delay		120		160		200		ns
t_{CWD}	$\overline{CAS}$ to write delay		70		95		125		ns
t_{RWL}	Write to $\overline{RAS}$ lead		50		70		85		ns
t_{CWL}	Write to $\overline{CAS}$ lead		50		70		85		ns
t_{WP}	Write duration		45		55		75		ns
t_{MOD}	Modify		0	9785	0	9715	0	9645	ns
t_{DS}[16]	Data set up		0		0		0		ns
t_{DH}[16]	Data hold		45		55		75		ns
t_{OFF}[14]	Output turn off delay		0	40	0	50	0	60	ns
t_{RAC}[12,13]	Row access		150		200		250		ns
t_{CAC}[11,12]	Column access		100		135		165		ns

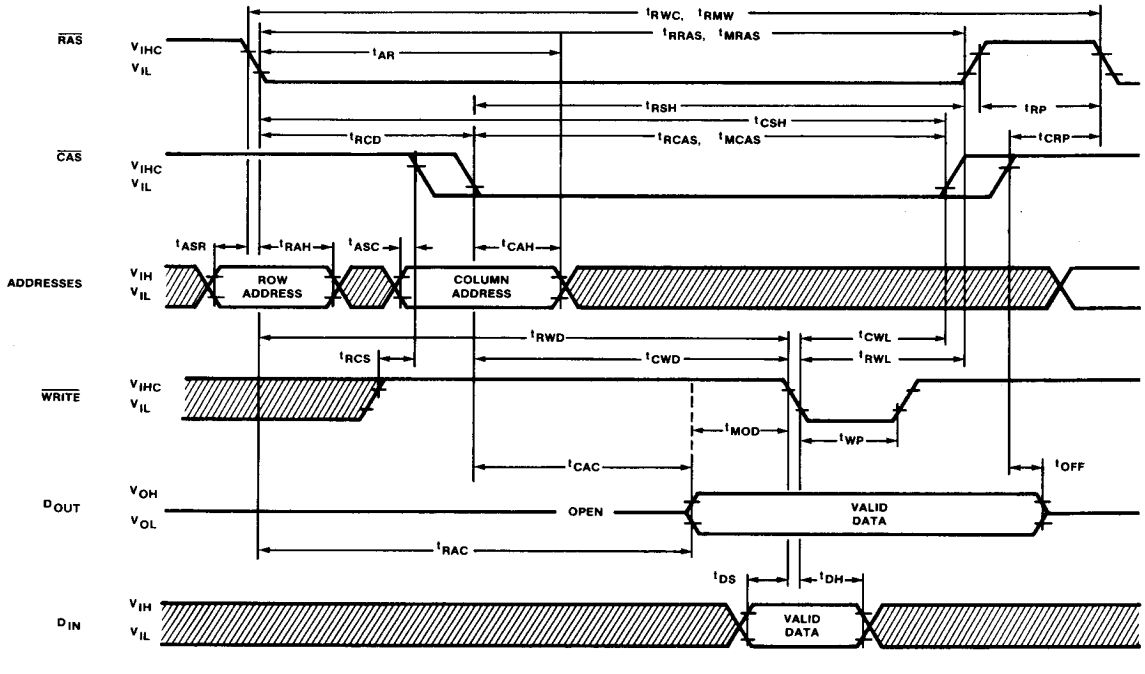
TIMING DIAGRAMS (Cont'd)

$\overline{RAS}$ ONLY REFRESH CYCLE



1. $\overline{CAS}$ = V_{IHC}
2. $\overline{WRITE}$ = Don't care

READ/WRITE, READ/MODIFY/WRITE CYCLE



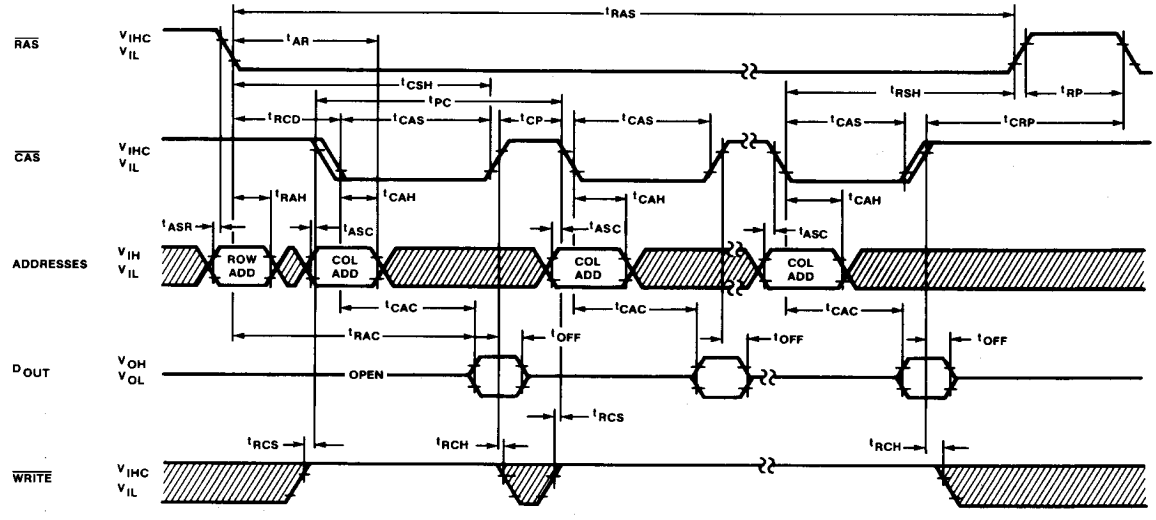
AC CHARACTERISTICS[7,8,9]

T_A = 0°C to +70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V unless otherwise specified.

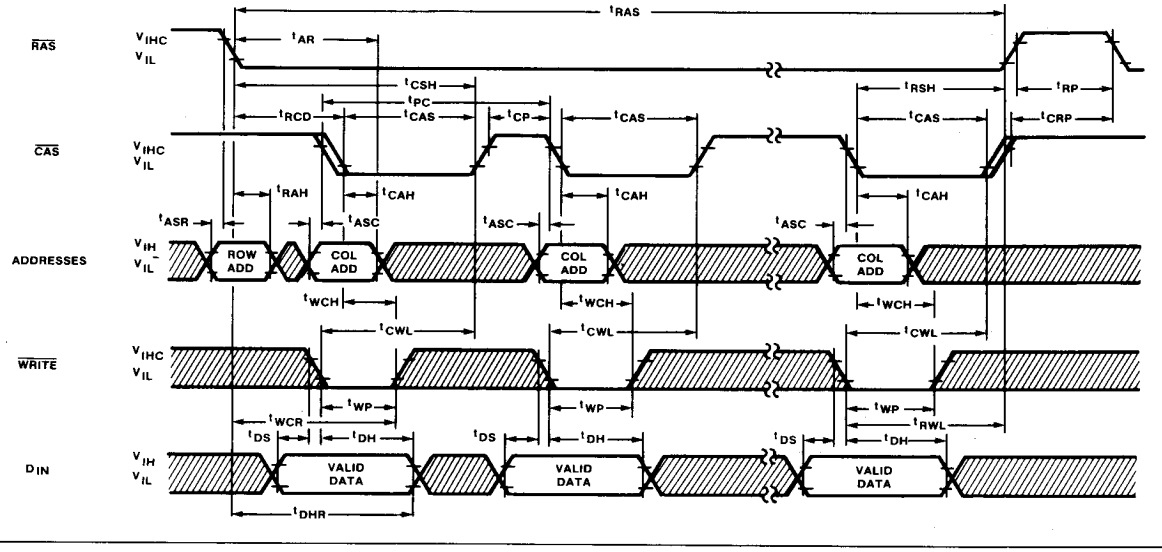
SYMBOL	PARAMETER	TEST CONDITIONS	2690-2		2690-3		2690-4		UNIT
			Min	Max	Min	Max	Min	Max	
	PAGE MODE CYCLES								
t_{REF}	Refresh			2		2		2	ms
t_T[9]	Transition		3	35	3	50	3	50	ns
t_{RAS}	$\overline{RAS}$ duration		150	10000	200	10000	250	10000	ns
t_{RP}	$\overline{RAS}$ precharge		100		120		150		ns
t_{RCD}[10]	Strobe delay		20	50	25	65	35	85	ns
t_{CAS}	$\overline{CAS}$ duration		100	10000	135	10000	165	10000	ns
t_{CP}	$\overline{CAS}$ HIGH duration		60		80		100		ns
t_{CSH}	$\overline{CAS}$ hold		150		200		250		ns
t_{PC}	Page mode cycle		170		225		275		ns
t_{RSH}	$\overline{RAS}$ hold		100		135		165		ns
t_{CRP}	$\overline{CAS}$ precharge		−20		−20		−20		ns
t_{ASR}	Row address set up		0		0		0		ns
t_{RAH}	Row address hold		20		25		35		ns
t_{ASC}	Column address set up		−10		−10		−10		ns
t_{CAH}	Column address hold		45		55		75		ns
t_{AR}	Address hold		95		120		160		ns
	PAGE MODE READ CYCLE								
t_{RCS}	Read set up		0		0		0		ns
t_{RCH}	Read hold		0		0		0		ns
t_{OFF}[14]	Output turn off delay		0	40	0	50	0	60	ns
t_{RAC}[12,13]	Row access		150		200		250		ns
t_{CAC}[11,12]	Column access		100		135		165		ns
t_{WCH}	Write hold		45		55		75		ns
t_{WP}	Write duration		45		55		75		ns
t_{CWL}	Write to $\overline{CAS}$ lead		50		70		85		ns
t_{RWL}	Write to $\overline{RAS}$ lead		50		70		85		ns
t_{WCR}	Write to $\overline{RAS}$ hold		95		120		160		ns
t_{DS}[16]	Data set up		0		0		0		ns
t_{DH}[16]	Data hold		45		55		75		ns
t_{DHR}	Data to $\overline{RAS}$ hold		95		120		160		ns

TIMING DIAGRAMS (Cont'd)

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



MOS MEMORY

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_M	Voltage on any pin with respect to V_{BB}	-0.5	20	V
V_{PM}	Voltage on V_{DD}, V_{CC} pins with respect to V_{SS}	-1.0	15	V
	$V_{BB} - V_{SS}$ ($V_{DD} > V_{SS}$)		0	V
	Temperature range			°C
T_A	Operating	0	+70	
T_{STG}	Storage	-55	+150	
I_{SSC}	Output current			mA
	Short circuit		50	
P_D	Power dissipation		1	W

DC ELECTRICAL CHARACTERISTICS[2]

T_A[3] = 0°C to +70°C, V_{DD} = 12V ±10%, V_{CC}[4] = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	Input voltage					V
V_{IL}	Low	Any input	-1.0		0.8	
V_{IH}	High	All inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7.0	
V_{IHC}	High	$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7		7.0	
	Output voltage[4]					V
V_{OL}	Low	I_{OL} = 4.2mA	0		0.4	
V_{OH}	High	I_{OH} = -5.0mA	2.4		V_{CC}	
	Leakage current					µA
I_{IL}	Input	Any input, V_{BB} = -5V, 0V < V_{IN} < 7V, All other pins not under test = 0V	-10		10	
I_{OL}	Output	D_{OUT} is disabled, 0V < V_{OUT} < 5.5V	-10		10	
	V_{DD} current[5]					mA
I_{DD1}	Operating	$\overline{RAS}$, $\overline{CAS}$ cycling			35	
I_{DD2}	Standby	$\overline{RAS}$ at V_{IHC}			1.5	
I_{DD3}	Refresh	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}			27	
I_{DD4}	Page mode	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling			27	
	Supply current					µA
I_{CC}	V_{CC}[6]					
I_{BB1}	Average V_{BB}	$\overline{RAS}$ and $\overline{CAS}$ cycling			200	
I_{BB2}	V_{BB}	$\overline{RAS}$ = V_{IHC}			100	
	Capacitance	Calculated from the equation $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3V				pF
C_{AD}	Address, D_{IN}				5	
C_C	$\overline{CAS}$, $\overline{RAS}$, $\overline{WRITE}$				10	
C_{OUT}	Output	$\overline{CAS}$ = V_{IHC} to disable D_{OUT}			7	

NOTES

1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages referenced to V_{SS}.
3. T_A is specified here for operation at frequencies to $t_{RC} \leq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible provided ac operating parameters are met, according to the following equation: T_A (max) °C = 70 - 9 X {cycle rate (MHz) - 2.66}.
4. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
5. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. I_{DD} limits at cycle rates other than those specified are determined by the following equations:

   For the 2690-2/2690-3:
   I_{DD1} (max) mA = 10 + 9.4 X cycle rate (MHz)
   I_{DD3} (max) mA = 10 + 6.5 X cycle rate (MHz)
   I_{DD4} (max) mA = 10 + 3.75 X cycle rate (MHz)

   For the 2690-4:
   I_{DD1} (max) mA = 10 + 10.25 X cycle rate (MHz)
   I_{DD3} (max) mA = 10 + 7 X cycle rate (MHz)
   I_{DD4} (max) mA = 10 + 4.7 X cycle rate (MHz)
6. I_{CC} depends upon output loading. During readout of high level data, V_{CC} is connected through a low impedance (135Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.