SSI 32R117/117R, 32R117A/117AR
2, 4, 6 Channel Read/Write Device

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July, 1990

DESCRIPTION

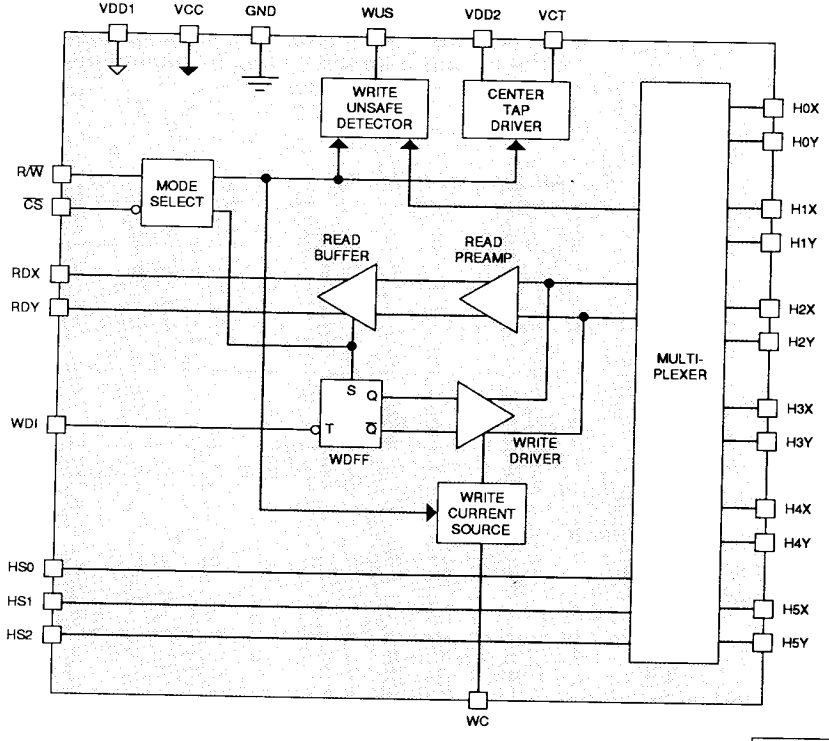
The SSI 32R117/117A devices are bipolar monolithic integrated circuits designed for use with center-tapped ferrite recording heads. They provide a low noise read path, write current control, and data protection circuitry for as many as six channels. The SSI 32R117/117A requires +5V and +12V power supplies and is available in 2, 4 or 6 channel versions with a variety of packages.

The SSI 32R117R/117AR differs from the SSI 32R117/117A by having internal damping resistors.

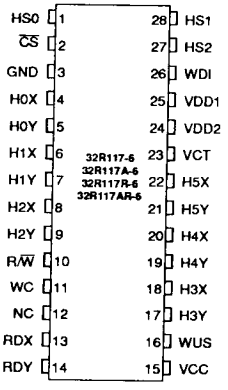
FEATURES

- **+5V, +12V power supplies**
- **Single or multi-platter Winchester drives**
- **Designed for center-tapped ferrite heads**
- **Programmable write current source**
- **Available in 2, 4 or 6 channels**
- **Easily multiplexed for larger systems**
- **Includes write unsafe detection**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R117/117A functions as a write driver or as a read amplifier for the selected head. Head selection and mode control are described in Tables 1 & 2. Both R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition.

WRITE MODE

The Write mode configures the SSI 32R117/117A as a current switch and activates the Write Unsafe Detector. Head current is toggled between the X- and Y-side of the recording head on the falling edges of WDI, Write Data Input. Note that a preceding read operation initializes the Write Data Flip-Flop, WDFF, to pass current through the X-side of the head. The magnitude of the write current, given by

Iw = K/Rwc, where K = Write Current Constant

is set by the external resistor, Rwc, connected from pin WC to GND.

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- Head open
- Head center tap open
- WDI frequency too low
- Device in Read mode
- Device not selected
- No write current

After the fault condition is removed, two negative transitions on WDI are required to clear WUS.

Power dissipation in write mode may be reduced by placing a resistor (RCT) between VDD1 & VDD2. The optimum resistor value is 130Ω x 50/Iw (Iw in mA). At low write currents (<15 mA) read mode dissipation is higher than write mode and RCT, though recommended, may not be considered necessary. In this case VDD2 is connected directly to VDD1.

READ MODE

In the Read mode the SSI 32R117/117A is configured as a low noise differential amplifier, the write current source and the write unsafe detector are deactivated, and the write data flip-flop is set. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. They should be AC coupled to the load.

Note that the internal write current source is deactivated for both the Read and the Chip Deselect mode. This eliminates the need for external gating of the write current source.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	x	Idle

TABLE 2: Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	x	None

0 = Low level 1 = High level x = Don't care

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0-HS2	I	Head Select: selects up to six heads
$\overline{CS}$	I	Chip Select: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects read mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition (open collector)
WDI	I	Write Data In: negative transition toggles the direction of the head current
H0X-H5X H0Y-H5Y	I/O	X,Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal out
WC	-	Write Current: used to set the magnitude of the write current
VCT	-	Voltage Center Tap: voltage source for head center tap
VCC	-	+5V
VDD1	-	+12V
VDD2	-	Positive power supply for the center tap voltage source
GND	-	Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ABSOLUTE MAXIMUM RATINGS (Operation above absolute maximum ratings may permanently damage the device. All voltages referenced to GND.)

PARAMETER		VALUE	UNITS
VDD1	DC Supply Voltage	-0.3 to +14	VDC
VDD2	DC Supply Voltage	-0.3 to +14	VDC
VCC	DC Supply Voltage	-0.3 to +6	VDC
VIN	Digital Input Voltage Range	-0.3 to VCC + 0.3	VDC
VH	Head Port Voltage Range	-0.3 to VDD + 0.3	VDC
Vwus	WUS Port Voltage Range	-0.3 to +14	VDC
Iw	Write Current	60	mA
Io	RDX, RDY Output Current	-10	mA
IVCT	VCT Output Current	-60	mA
Iwus	WUS Output Current	+12	mA
Tstg	Storage Temperature Range	-65 to +150	°C
Lead Temperature, PDIP, Flatpack (10 sec soldering)		260	°C
Package Temperature, PLCC, SOL (20 sec reflow)		215	°C

RECOMMENDED OPERATION CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DC Supply Voltage	VDD1		10.8	12.0	13.2	VDC
DC Supply Voltage	VCC		4.5	5.0	5.5	VDC
Head Inductance	Lh		5		15	µH
Damping Resistor	RD	32R117 only	500		2000	Ω
RCT Resistor	RCT		125.0	130	135.0	Ω
Write Current	Iw		25		50	mA
Junction Temperature Range	Tj		25		125	°C

DC CHARACTERISTICS
(Unless otherwise specified, recommended operating conditions apply.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VCC Supply Current		Read/Idle Mode			25	mA
		Write Mode			30	mA
VDD Supply Current		Idle Mode			25	mA
		Read Mode			50	mA
		Write Mode			30+Iw	mA
Power Dissipation (Tj = +125°C)		Idle Mode			400	mW
		Read Mode			600	mW
		Write Mode, Iw = 50 mA, RCT = 130Ω			700	mW
		Write Mode, Iw = 50 mA, RCT = 0Ω			1050	mW
Digital Inputs						
Input Low Voltage	VIL		-0.3		0.8	VDC
Input High Voltage	VIH		2.0		VCC+0.3	VDC
Input Low Current	IIL	VIL = 0.8V	-0.4			mA
Input High Current	IIH	VIH = 2.0V			100	µA
WUS Output	VOL	IOL = 8 mA			0.5	VDC
WUS Output	IOH	VOH = 5.0V			100	µA
Center Tap Voltage	VCT	Write Mode		6.0		VDC
		Read Mode		4.0		VDC

WRITE CHARACTERISTICS (Unless otherwise specified: recommended operating conditions apply, IW = 45 mA, Lh = 10 µH, Rd = 750Ω (32R117/A only), f(Data) = 5 MHz, CL(RDX, RDY) ≤ 20 pF)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Write Current Range		10		50	mA
Write Current Constant "K"		133		147	V
Differential Head Voltage Swing		8.0			V(pk)
Unselected Head Transient Current				2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	32R117/A	10K			Ω
	32R117R	562		938	Ω
	32R117/AR	638		863	Ω
WDI Transition Frequency	WUS = low	250			KHz
Iwc to Head Current Gain	Iw/Iwc		20		mA/mA
Unselected Head Leakage Current	Sum of X & Y side leakage current			85	µA

READ CHARACTERISTICS
(Unless otherwise specified: recommended operating conditions apply, IW = 45 mA, Lh = 10 µH, Rd = 750Ω (32R117/117A only), f(Data) = 5 MHz, CL(RDX, RDY) ≤ 20 pF, Vin is referenced to VCT)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain	Vin = 1 mVpp @ 300 KHz RL(RDX), RL(RDY) = 1 KΩ 32R117/117R	80		120	V/V
	32R117/117AR	90		110	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%, Vin = Vi + 0.5 mVpp @ 300 KHz	-3		+3	mV
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0 32R117/R			2.1	nV/√Hz
	32R117A/AR			1.7	nV/√Hz
Differential Input Capacitance	f = 5 MHz			20	pF
Differential Input Resistance	32R117/117A, f = 5 MHz	2K			Ω
	32R117R, f = 5 MHz	390		810	Ω
	32R117/117AR	450		750	Ω

READ CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Input Bias Current (per side)				45	µA
Common Mode Rejection Ratio	Vcm = VCT + 100 mVpp @ 5 MHz	50			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1, VDD2 or VCC	45			dB
Channel Separation	Unselected Channels: Vin=100 mVpp @ 5 MHz; Selected Channel: Vin = 0 mVpp	45			dB
Output Offset Voltage	32R117/117R	-480		+480	mV
	32R117/117AR	-440		+440	mV
Common Mode Output Voltage	Read Mode	5		7	V
	Write/Idle Mode		4.3		V
Single Ended Output Resistance	f = 5 MHz			30	Ω
Leakage Current, RDX, RDY	RDX, RDY = 6V Write/Idle Mode	-100		+100	µA
Output Current	AC Coupled Load, RDX to RDY	2			mA

SWITCHING CHARACTERISTICS (Unless otherwise specified: recommended operating conditions apply, IW = 45 mA, Lh = 10 µH, Rd = 750Ω (32R117/A) only, f(Data) = 5 MHz)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$ To Write	Delay to 90% of write current			1.0	µs
R/$\overline{W}$ to Read	Delay to 90% of 100 mV 10 MHz read signal envelope or to 90 % decay of write current			1.0	µs
$\overline{CS}$ to Select	Delay to 90% of write current or to 90% of 100mV 10MHz read signal envelope			1.0	µs
$\overline{CS}$ to Unselect	Delay to 90% decay of write current			1.0	µs

SWITCHING CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
HS0 - HS2 to any head	Delay to 90% of 100 mV 10 MHz read signal envelope			1.0	µs
WUS - Safe to Unsafe - TD1	Iw = 50 mA	1.6		8.0	µs
WUS - Unsafe to Safe - TD2	Iw = 20 mA			1.0	µs
Head Current (Lh = 0 µH, Rh = 0Ω)					
Prop. Delay - TD3	From 50% points			25	ns
Asymmetry	WDI has 50% duty cycle and 1ns rise/fall time			2	ns
Rise/Fall Time	10% - 90% points			20	ns

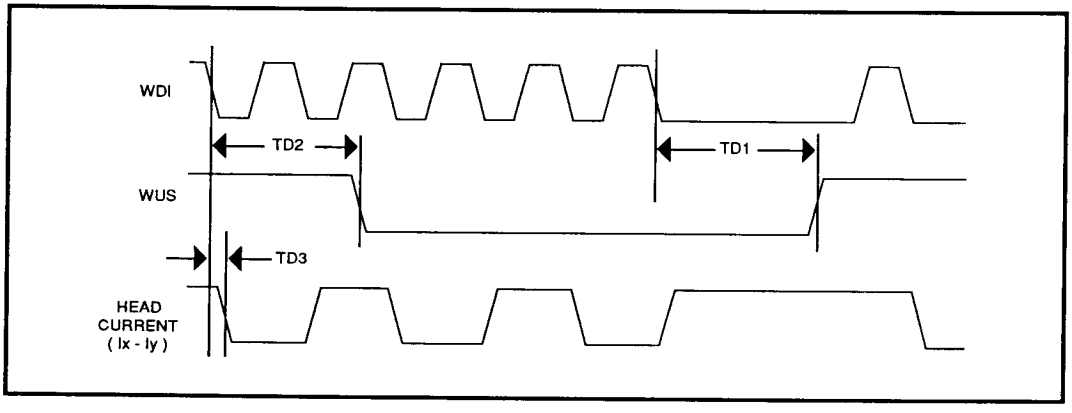
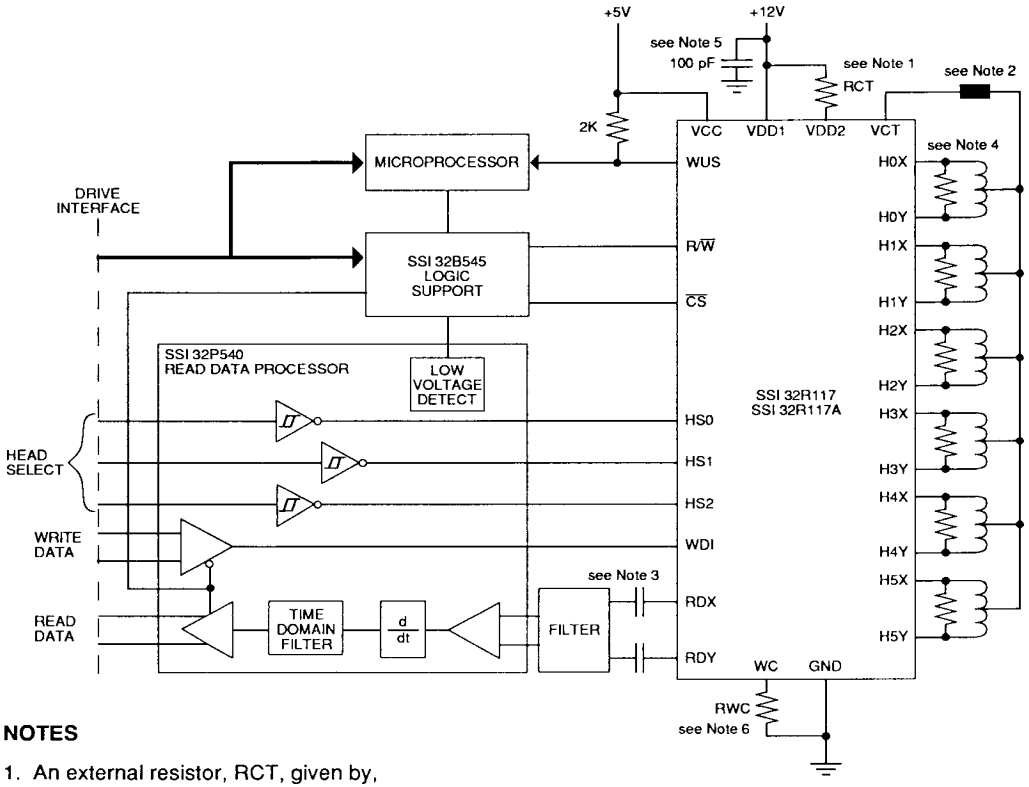


FIGURE 1: Write Mode Timing Diagram



NOTES

1. An external resistor, RCT, given by,

   117/117R RCT = 130(55/Iw)Ω, where Iw is in mA,

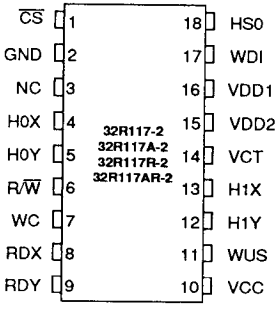
   117/117AR = 130(50/Iw)Ω

   can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. A ferrite bead (Ferroxcube 5659065/4A6) can be used to suppress write current overshoot and ringing induced by flex cable parasitics.
3. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF.
4. Damping resistors not required on 32R117R/117AR version.
5. The power bypassing capacitor must be located close to the 32R117/117A with its ground returned directly to device ground with as short a path as possible.
6. To reduce ringing due to stray capacitance this resistor should be located close to the 32R117/117A. Where this is not desirable a series resistor can be used to buffer a long WC line.

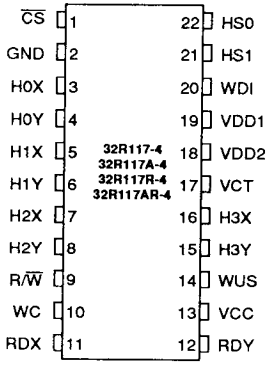
FIGURE 2: Applications Information

PACKAGE PIN DESIGNATIONS

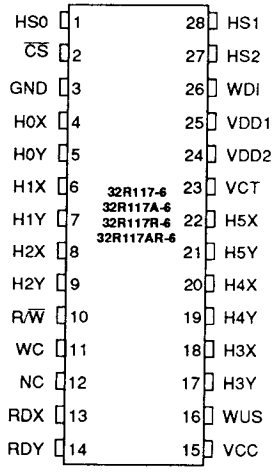
(TOP VIEW)



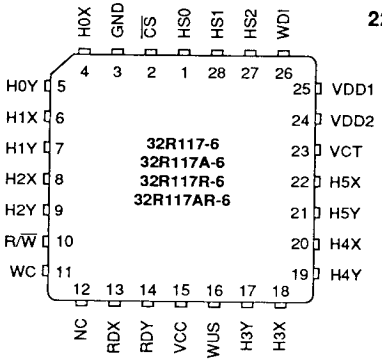
18-lead PDIP



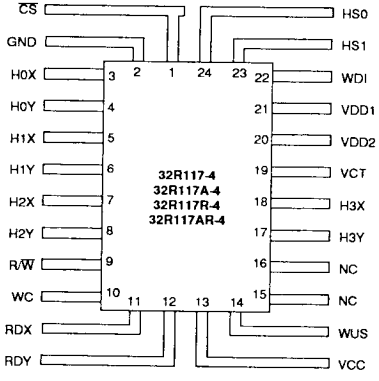
22-lead PDIP



28-lead PDIP,
Flatpack, SOL



28-lead PLCC



24-lead Flatpack, SOL

THERMAL CHARACTERISTICS

PACKAGE	Øja
18-lead PDIP	140°C/W
22-lead PDIP	65°C/W
24-lead Flatpack	110°C/W
SOL	80°C/W
28-lead PDIP	55°C/W
Flatpack	100°C/W
PLCC	65°C/W
SOL	70°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R117		
2-Channel PDIP	SSI 32R117-2P	32R117-2P
4-Channel PDIP	SSI 32R117-4CP	32R117-4CP
4-Channel SOL	SSI 32R117-4CL	32R117-4CL
4-Channel Flatpack	SSI 32R117-4F	32R117-4F
6-Channel PDIP	SSI 32R117-6CP	32R117-6CP
6-Channel SOL	SSI 32R117-6CL	32R117-6CL
6-Channel Flatpack	SSI 32R117-6F	32R117-6F
6-Channel PLCC	SSI 32R117-6CH	32R117-6CH
SSI 32R117R with Internal Damping Resistor		
2-Channel PDIP	SSI 32R117R-2P	32R117R-2P
4-Channel PDIP	SSI 32R117R-4CP	32R117R-4CP
4-Channel SOL	SSI 32R117R-4CL	32R117R-4CL
4-Channel Flatpack	SSI 32R117R-4F	32R117R-4F
6-Channel PDIP	SSI 32R117R-6CP	32R117R-6CP
6-Channel SOL	SSI 32R117R-6CL	32R117R-6CL
6-Channel Flatpack	SSI 32R117R-6F	32R117R-6F
6-Channel PLCC	SSI 32R117R-6CH	32R117R-6CH
SSI 32R117A		
2-Channel PDIP	SSI 32R117A-2P	32R117A-2P
4-Channel PDIP	SSI 32R117A-4CP	32R117A-4CP
4-Channel SOL	SSI 32R117A-4CL	32R117A-4CL
4-Channel Flatpack	SSI 32R117A-4F	32R117A-4F
6-Channel PDIP	SSI 32R117A-6CP	32R117A-6CP
6-Channel SOL	SSI 32R117A-6CL	32R117A-6CL
6-Channel Flatpack	SSI 32R117A-6F	32R117A-6F
6-Channel PLCC	SSI 32R117A-6CH	32R117A-6CH
SSI 32R117AR with Internal Damping Resistor		
2-Channel PDIP	SSI 32R117AR-2P	32R117AR-2P
4-Channel PDIP	SSI 32R117AR-4CP	32R117AR-4CP
4-Channel SOL	SSI 32R117AR-4CL	32R117AR-4CL
4-Channel Flatpack	SSI 32R117AR-4F	32R117AR-4F
6-Channel PDIP	SSI 32R117AR-6CP	32R117AR-6CP
6-Channel SOL	SSI 32R117AR-6CL	32R117AR-6CL
6-Channel Flatpack	SSI 32R117AR-6F	32R117AR-6F
6-Channel PLCC	SSI 32R117AR-6CH	32R117AR-6CH

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