

TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD × 8 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS

TMM2088P-35, TMM2088P-45

DESCRIPTION

The TMM2088P is a 65,536 bits high speed N-channel silicon gate MOS static random access memory organized as 8,192 words by 8 bits and operates from a single 5-volt supply. The TMM2088P features an automatic stand-by mode when deselected by $\overline{CS1}$ signal. Thus the TMM2088P is suitable for use in cache memory and high speed storage. The TMM2088P is offered in a 28 pin standard plastic dual in-line package with 0.3 inch width for high density assembly.

FEATURES

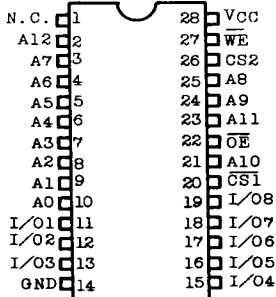
• Access Time and Current

Parameter Part Number	Access Time (MAX.)	Operating Current (MAX.)	Standby Current (MAX.)
TMM2088P-35	35ns	135mA	15mA
TMM2088P-45	45ns	135mA	15mA

• Inputs Protected: (All inputs have protection against static charge.)

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature: ($\overline{CS1}$)
- Output Buffer Control: (\overline{OE})
- Three State Outputs
- All Inputs and Outputs: (Directly TTL Compatible)

PIN CONNECTION



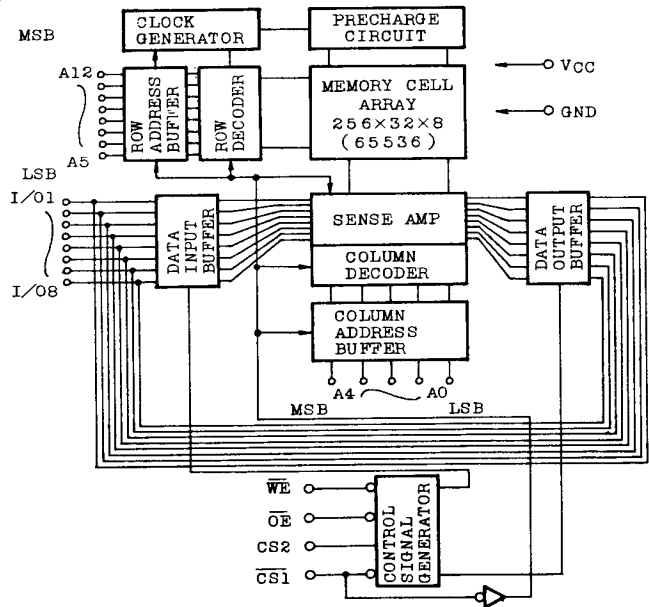
PIN NAMES

AO ~ A12	Address Inputs
WE	Write Enable Input
OE	Output Enable Input
CS1, CS2	Chip Select Inputs
I/O1 ~ I/O8	Data Input/Output
VCC	Power (+5V)
GND	Ground
N.C.	No Connection

OPERATION MODE

MODE	CS1	CS2	OE	WE	I/O1 ~ 8	Power
Write	L	H	*	L	In	Active
Read	L	H	L	H	Out	Active
Standby	H	*	*	*	High-Z	Standby
Standby	L	L	*	*	High-Z	Active
Output Buffer Disable	L	H	H	H	High-Z	Active

BLOCK DIAGRAM



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MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	Power Supply Voltage	-3.5 ~ 7.0	V
V _{IN} , V _{OUT}	Input Output Voltage	-3.5 ~ 7.0	V
T _{opr.}	Operating Temperature	0 ~ 70	°C
T _{stg.}	Storage Temperature	-55 ~ 150	°C
T _{solder}	Soldering Temperature · Time	260 · 10	°C·sec
P _D	Power Dissipation (Ta=70°C)	1.0	W

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	-	V _{CC} +1.0	V
V _{IL}	Input Low Voltage	-3.0*	-	0.8	V
V _{CC}	Supply Voltage	4.5	5.0	5.5	V

* Pulse Width: 10ns, DC: -0.5V (Min.)

D.C. CHARACTERISTICS (Ta=0 ~ 70°C, V_{CC}=5.0V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I _{IIL}	Input Leakage Current	V _{IN} =0V ~ 5.5V	-1.0	1.0	μA
I _{OH}	Output High Current	V _{OH} =2.4V	-4.0	-	mA
I _{OL}	Output Low Current	V _{OL} =0.4V	8.0	-	mA
I _{LO}	Output Leakage Current	$\overline{CS1}=V_{IH}$ or CS2=V _{IL} or $\overline{WE}=V_{IL}$ or $\overline{OE}=V_{IH}$, V _{OUT} =0V~5.5V	-1.0	1.0	μA
I _{SBP}	Peak Power-on Current	$\overline{CS1}=V_{CC}$, CS2=0V, I _{OUT} =0mA	-	30	mA
I _{SB}	Standby Current	$\overline{CS1}=V_{IH}$, I _{OUT} =0mA	-	15	mA
I _{CC}	Operating Current	$\overline{CS1}=V_{IL}$, I _{OUT} =0mA	-	135	mA

CAPACITANCE* (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} =0V	8	pF
C _{OUT}	Output Capacitance	V _{IN} =0V	10	pF

* Note: This parameter is periodically sampled and is not 100% tested.

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A.C. CHARACTERISTICS (Ta=0 ~ 70°C, VCC=5V±10%)

READ CYCLE

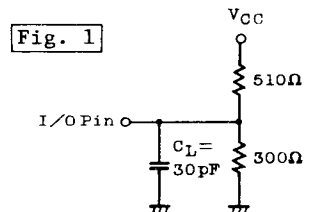
SYMBOL	PARAMETER	TMM2088P-35		TMM2088P-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	35	-	45	-	ns
t _{ACC}	Address Access Time	-	35	-	45	
t _{CO1}	CS1 Access Time	-	35	-	45	
t _{CO2}	CS2 Access Time	-	25	-	25	
t _{OE}	OE Access Time	-	20	-	20	
t _{OH}	Output Data Hold Time from Address Change	5	-	5	-	
t _{CLZ}	Output Enable Time from CS1 or CS2	0	-	5	-	
t _{CHZ}	Output Disable Time from CS1 or CS2	-	20	-	20	
t _{OLZ}	Output Enable Time from OE	0	-	0	-	
t _{OHZ}	Output Disable Time from OE	-	15	-	15	
t _{PU}	Chip Selection to Power Up Time	0	-	0	-	
t _{PD}	Chip Deselection to Power Down Time	-	30	-	30	

WRITE CYCLE

SYMBOL	PARAMETER	TMM2088P-35		TMM2088P-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	35	-	45	-	ns
t _{CW}	Chip Selection to End of Write	30	-	40	-	
t _{AS}	Address Set Up Time	0	-	0	-	
t _{WP}	Write Pulse Width	25	-	35	-	
t _{WR}	Write Recovery Time	0	-	0	-	
t _{DS}	Data Set Up Time	15	-	20	-	
t _{DH}	Data Hold Time	0	-	0	-	
t _{WLZ}	Output Enable Time from WE	0	-	0	-	
t _{WHZ}	Output Disable Time from WE	-	15	-	15	

A.C. TEST CONDITIONS

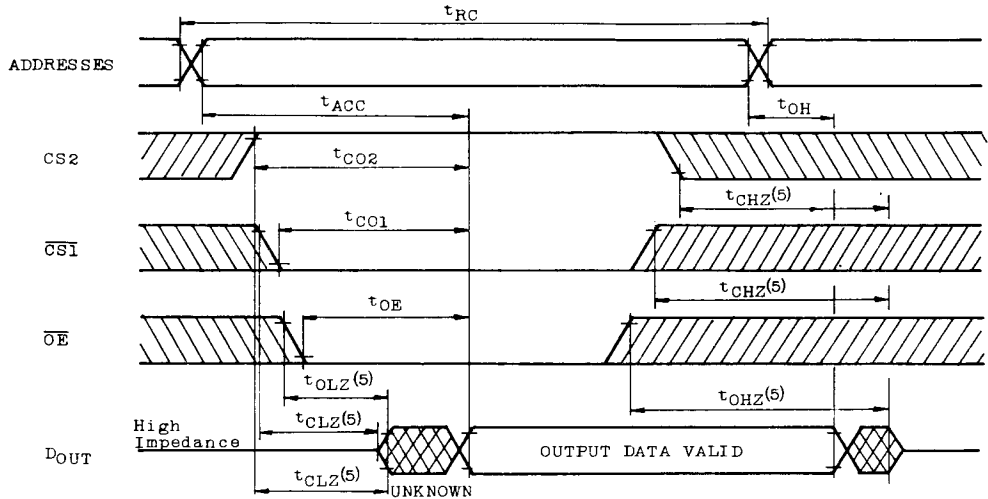
Input Pulse Levels	0.0 ~ 3.0V
Input Rise and Fall Time	5ns
Input and Output Reference Levels	2.0V/0.8V
Output Load	Fig. 1



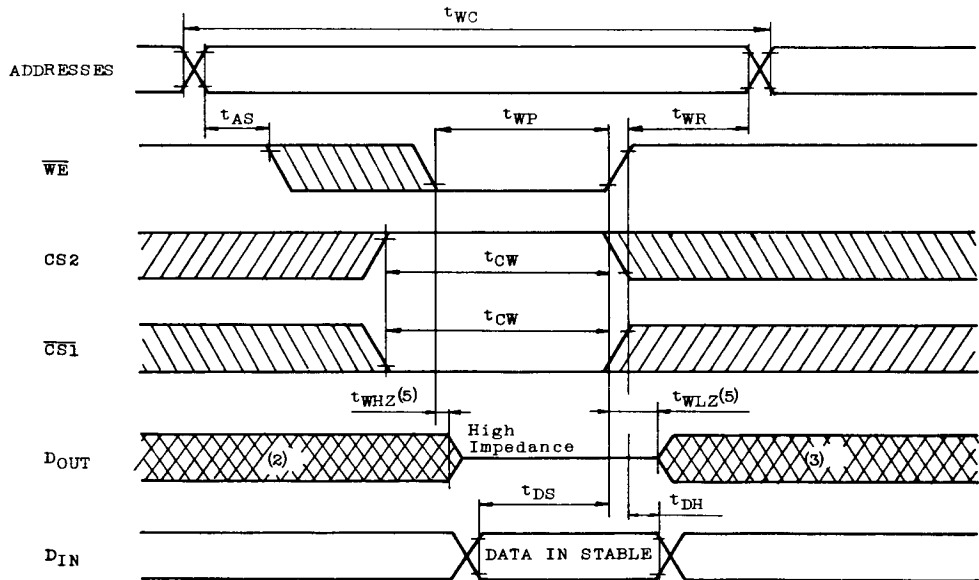
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TIMING WAVEFORMS

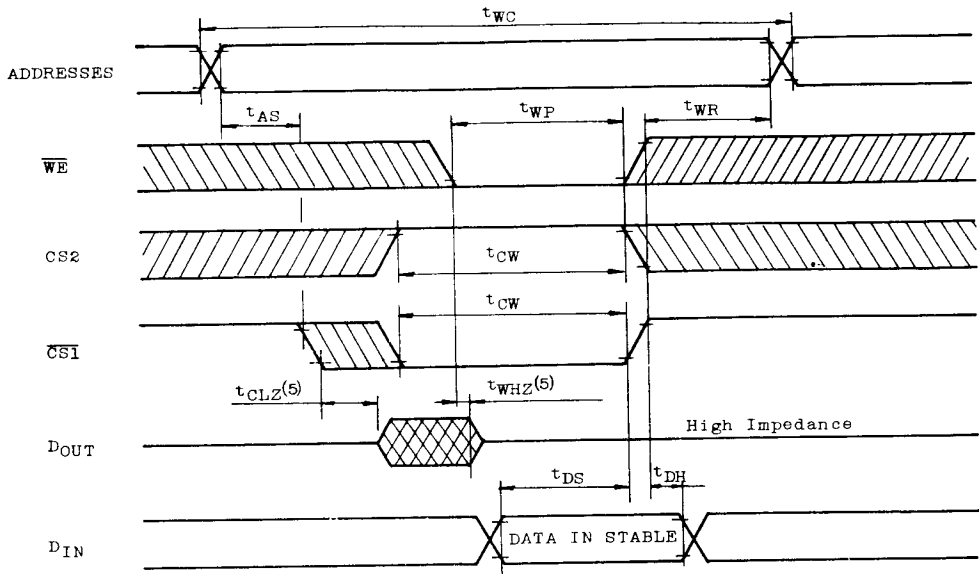
READ CYCLE (1)



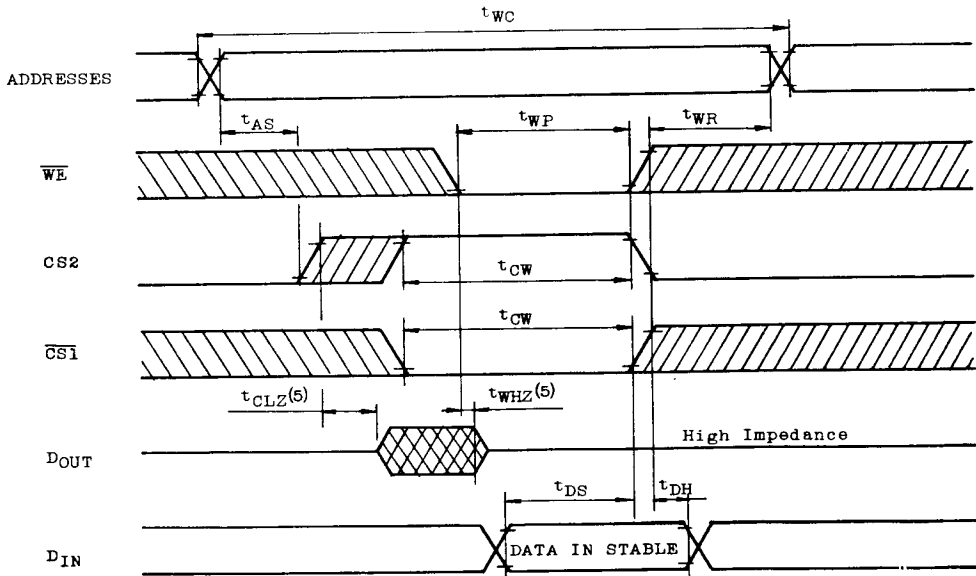
WRITE CYCLE 1 (4) (\overline{WE} Controlled Write)



WRITE CYCLE 2 (4) ($\overline{\text{CS1}}$ Controlled Write)



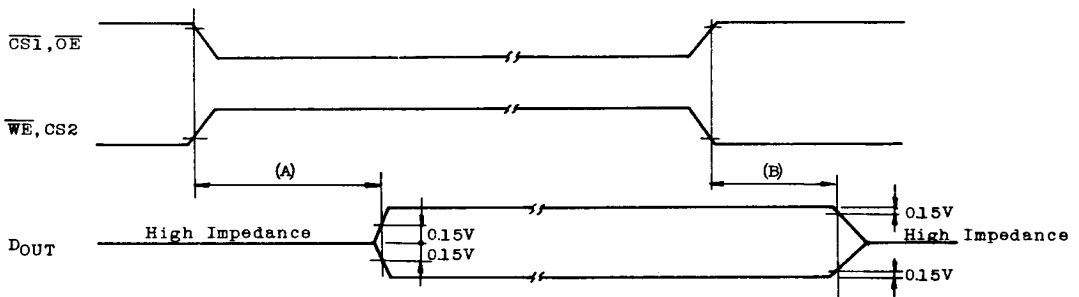
WRITE CYCLE 3 (4) (CS2 Controlled Write)



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- Note: 1. \overline{WE} is High for Read Cycle.
2. Assuming that $\overline{CS1}$ Low transition or CS2 High transition occurs coincident with or after \overline{WE} Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CS1}$ High transition or CS2 Low transition occurs coincident with or prior to \overline{WE} High transition, Outputs remain in a high impedance state.
4. Assuming that \overline{OE} is High for Write Cycle, Outputs are in high impedance state during this period.
5. These parameters are specified as follows and measured by using the load shown in Fig. 1.

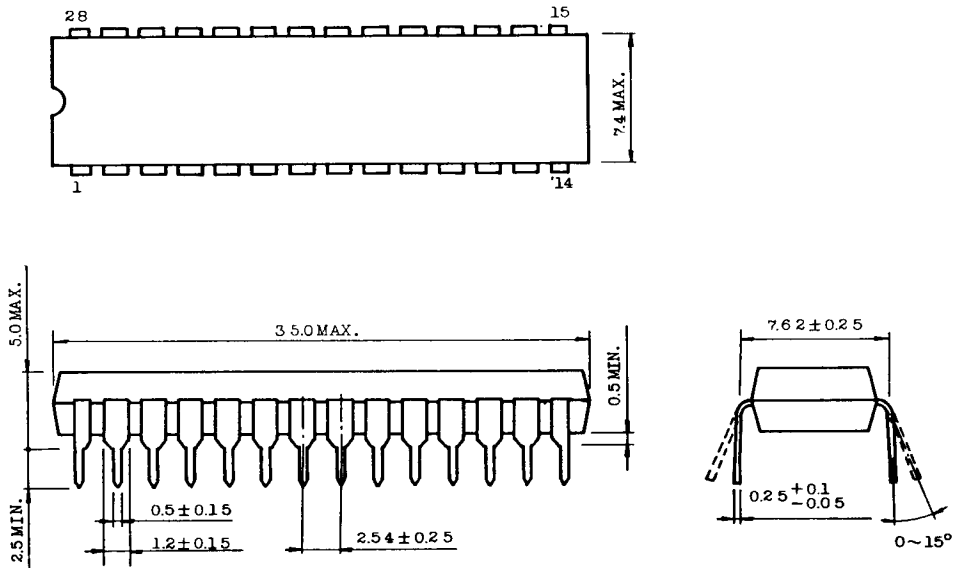
- (A) t_{CLZ} , t_{OLZ} , t_{WLZ} Output Enable Time
- (B) t_{CHZ} , t_{OHZ} , t_{WHZ} Output Disable Time



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DIP 28 PIN OUTLINE DRAWING

Unit in mm



Note: Lead pitch is 2.54 and tolerance is ± 0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.