TMS 4003 JR, TMS 4003 NC
256-BIT RANDOM-ACCESS MEMORY

FEBRUARY, 1971

FOR MEMORY APPLICATIONS REQUIRING HIGH-SPEED READ/WRITE CAPABILITY

- **Nondestructive readout**
- **Static operation**
- **System access time under 200 ns**
- **Low power dissipation**

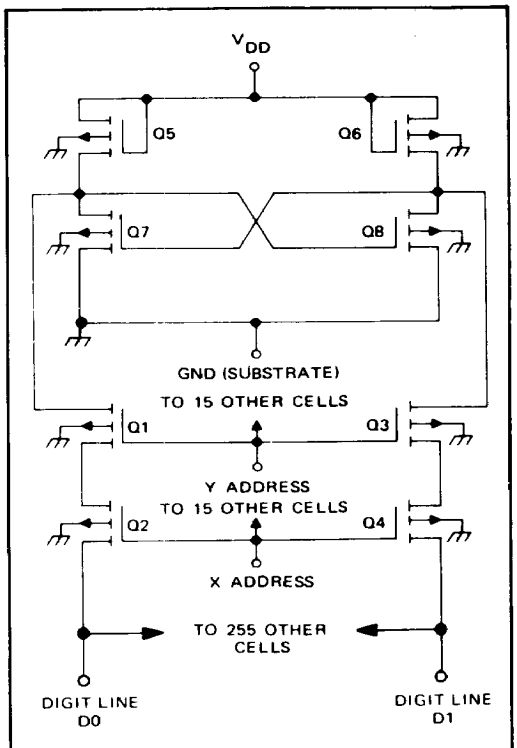
description

The TMS 4003 JR/NC is a high-speed random-access memory consisting of 256 cross-coupled flip-flops organized as 256 one-bit words. The entire device is constructed on a single monolithic chip using thick-oxide techniques to produce MOS P-channel enhancement-type transistors. Active-element design permits nondestructive readout, because addressing each bit tends to reinforce its existing state. Digit lines can be wire-OR connected to obtain memory planes greater than 256 words. External decoding circuitry can be used for additional planes to achieve desired word length. Selection of a given bit for reading or writing is accomplished by the coincident addressing of one of 16 X lines and one of 16 Y lines. These two lines are taken to V_{DD} while all other X and Y lines are held at ground.

Memory writing is accomplished by externally addressing the desired cell and bringing the appropriate digit line to ground while holding the other digit line at its nominal V_{DD} potential.

Reading an addressed cell requires sensing a differential current between the two digit lines. Both digit lines should be held near their nominal value of V_{DD}. This causes addressing transistors Q1, Q2, Q3, and Q4 to act as additional load resistors in parallel with standby load resistors Q5 and Q6, (see Figure 1). Depending on the flip-flop state, current will flow in one of the digit lines and not the other.

Maximum speed of the circuit is limited by the propagation delay of the Y address voltage through a series of P-diffused tunnels. The write or read cycle time, including this delay and the TTL address-decode delay, will be under 200 nanoseconds (see Figure 2).



CELL SCHEMATIC (1 OF 256 CELLS)

FIGURE 1

Power dissipation is typically 0.6 mW per bit when the memory is operated with an 18-volt dc power supply. Significantly lower average power dissipation may be obtained without sacrifice of system performance by synchronously or asynchronously pulsing the V_{DD} power supply. This feature is a result of the temporary data storage provided by the gate capacitance of transistors Q7 and Q8.

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description (continued)

A unit mounted in a 40-pin hermetically sealed ceramic dual-in-line package is designated "TMS 4003 JR". Mounted in a 40-pin plastic dual-in-line package the device is numbered "TMS 4003 NC".

logic

Logic levels for this memory are defined in terms of standard NEGATIVE LOGIC where:

−16 V to −20 V = LOGICAL 1
+0.3 V to −2 V = LOGICAL 0

OPERATING MODE	ADDRESS LINES OF SELECTED CELL		DIGIT-LINE TERMINALS	
	X	Y	D1	D0
Read	1	1	1	1
Write a zero	1	1	1	0
Write a one	1	1	0	1

A selected cell has both its X and Y address lines at logical 1. During read and write operations, only one cell should be selected at a time. An unselected cell is a cell which has at least one of its address lines at logical 0.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage at any terminal relative to substrate (GND) . . . . . +0.3 V to −22 V
Operating free-air temperature range . . . . . −55°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNIT
Supply voltage V_{DD}	−16	−18	−20	V
Write access time, t_{aw} (See Note 1 and Figure 3)	80			ns
Write pulse width, t_{pw} (See Figure 3)	30			ns

NOTE: 1. Write access time is the delay between the application of address voltages at the X and Y inputs and the start of the write pulse. Premature application of the write pulse may cause undesired writing into cells other than the addressed cell.

operating characteristics (unless otherwise noted T_A = 25°C)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Read-mode sense current	$V_{Xn} = V_{Ym} = V_{in(D0)} = V_{in(D1)} = V_{DD} = -16$ V, Logical 0 stored in cell nm	D0	−200	−400		μA
		D1		−0.1	−10	
	$V_{Xn} = V_{Ym} = V_{in(D0)} = V_{in(D1)} = V_{DD} = -16$ V, Logical 1 stored in cell nm	D0		−0.1	−10	
		D1	−200	−400		
	$V_{Xn} = V_{Ym} = V_{in(D0)} = V_{in(D1)} = V_{DD} = -18$ V, Logical 0 stored in cell nm	D0	−300	−500		
		D1		−0.1	−10	
	$V_{Xn} = V_{Ym} = V_{in(D0)} = V_{in(D1)} = V_{DD} = -18$ V, Logical 1 stored in cell nm	D0		−0.1	−10	
		D1	−300	−500		
Address-line current (16 lines in parallel)	V_X or V_Y = −20 V, $V_{in(D0)} = V_{in(D1)} = V_{DD} = 0$ V				−10	μA
Total power dissipation	One cell addressed, V_{DD} = −18 V			150	300	mW
	One cell addressed, V_{DD} = −20 V, T_A = −55°C				500	

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operating characteristics, continued (unless otherwise noted $V_{DD} = -18$ V, $T_A = 25°C$)

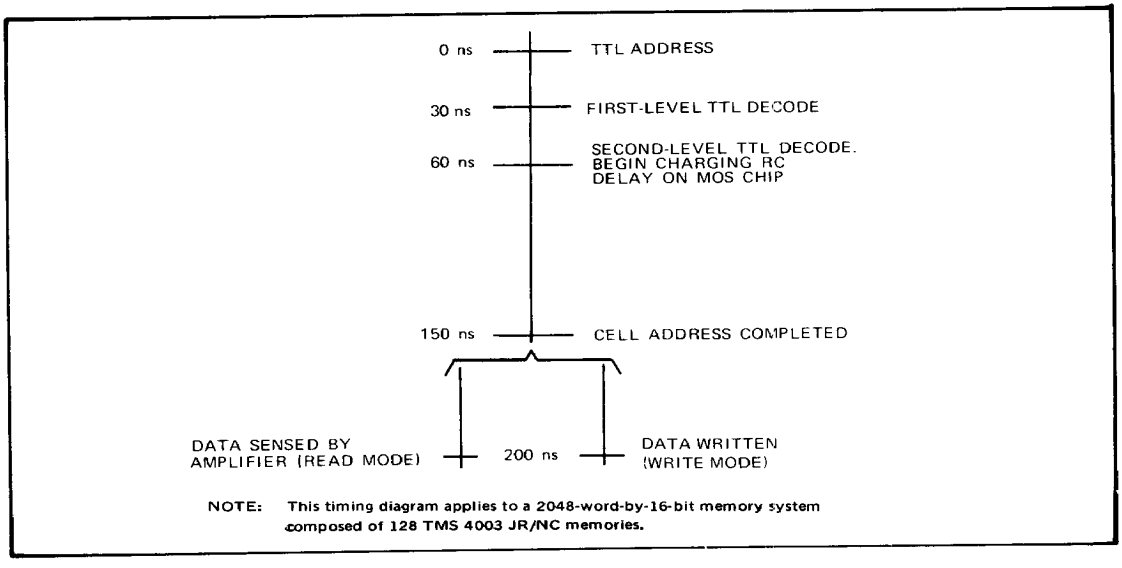
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Capacitance between digit-line terminal and substrate	$V_{in(D0)} = V_{in(D1)} = 0$ V, f = 140 kHz, $V_X = V_Y = 0$ V (or one cell addressed), See Note 2		50		pF
	$V_{in(D0)} = V_{in(D1)} = -18$ V, f = 140 kHz, $V_X = V_Y = 0$ V (or one cell addressed), See Note 2		30		
Capacitance between digit-line terminal and physically adjacent address terminal (D0-to-X2 or D1-to-Y1, see Note 3)	$V_{in(D0)} = V_{in(X2)} = 0$ to -18 V, $V_{in(D1)} = V_{in(Y1)} = 0$ to -18 V, f = 140 kHz, See Note 2		8†		pF
Capacitance between address terminal and substrate	$V_X = V_Y = 0$ to -18 V, f = 140 kHz, See Note 2		8†		pF
Capacitance between V_{DD} terminal and substrate	$V_{DD} = V_X = V_Y = 0$ to -18 V, f = 140 kHz, See Note 2		50†		pF
Read access time, t_{ar} (see Note 4)	See Figure 3, $R_L = 51\ \Omega$		30	60	ns

NOTES: **2. All capacitances are measured with all other elements ac grounded.**

3. Typical capacitance between digit-line terminals and all other address lines will be less than that shown for the adjacent address lines.

4. Read access time is the delay between the application of address voltages at the X and Y inputs and the availability of differential current between the digit lines.

†These typical values are the average for the voltage range 0 to -18 V.



NOTE: This timing diagram applies to a 2048-word-by-16-bit memory system composed of 128 TMS 4003 JR/NC memories.

FIGURE 2 – TYPICAL SYSTEM CYCLE TIME

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PARAMETER MEASUREMENT INFORMATION

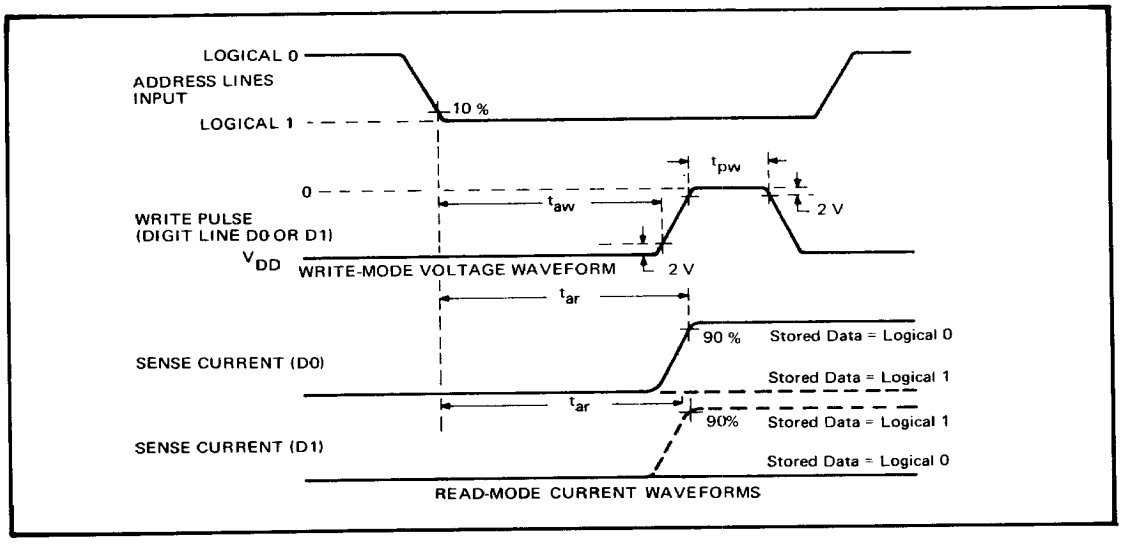

FIGURE 3 – TYPICAL SWITCHING WAVEFORMS

TYPICAL CHARACTERISTICS

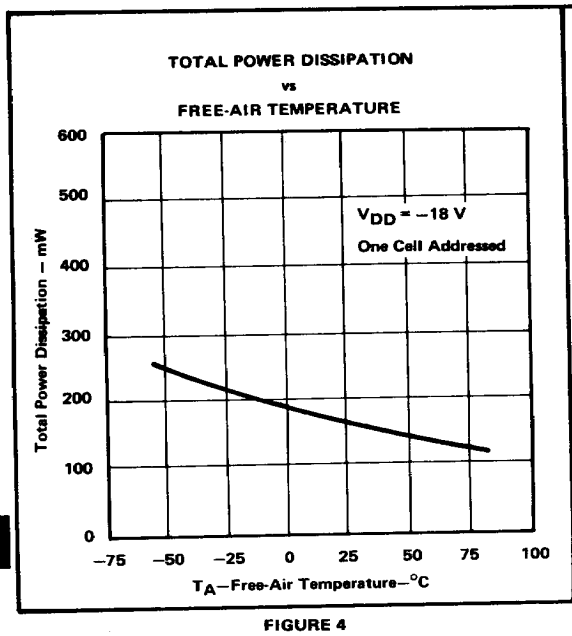

FIGURE 4

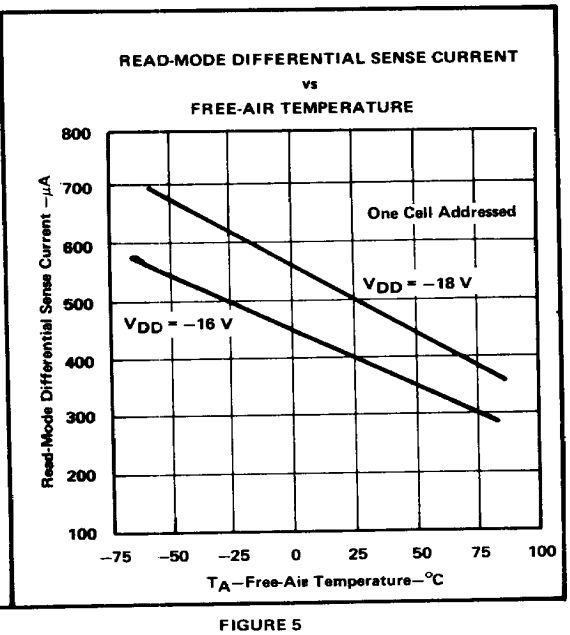

FIGURE 5

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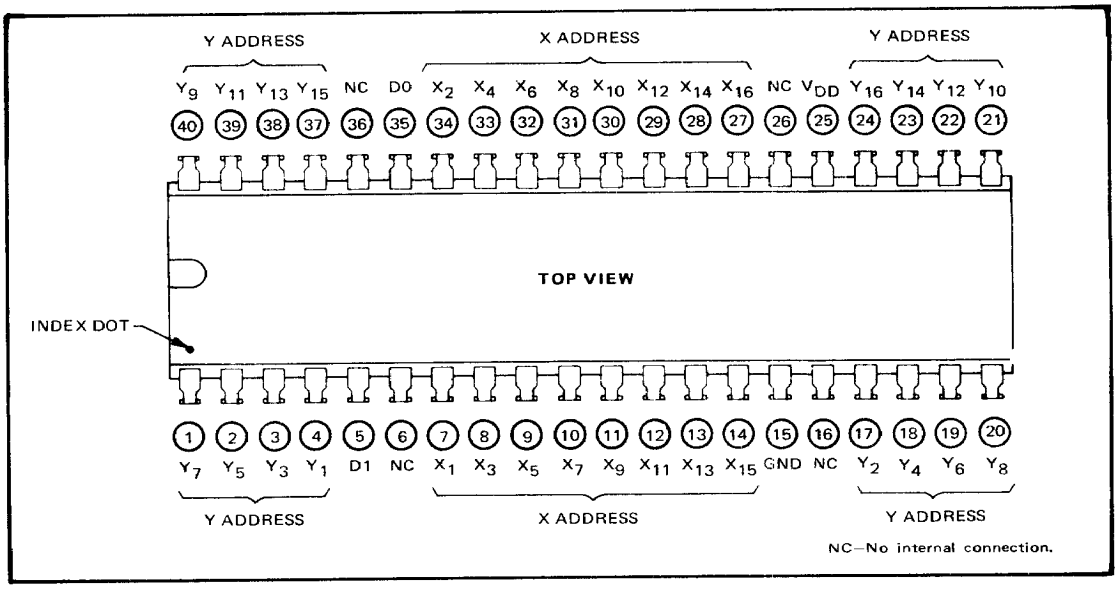
mechanical data and pin configuration

The device is available in both a 40-pin hermetically sealed ceramic dual-in-line package (TMS 4003 JR) and a 40-pin plastic dual-in-line package (TMS 4003 NC). These packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)



TYPICAL APPLICATION DATA

An actual negative supply for V_{DD} is not necessary. The V_{DD} terminal can be returned to system ground with a positive potential equal in magnitude to the voltage specified for V_{DD} applied to device ground (pin 15). This simplifies external circuitry, particularly when using bipolar systems such as TTL. The MOS device ground V_{SS}, is nominally +18 V while the V_{DD} terminal is at system ground. Addressing occurs when one X-address line and one Y-address line are pulled to ground. Unselected address lines should remain at V_{SS}.

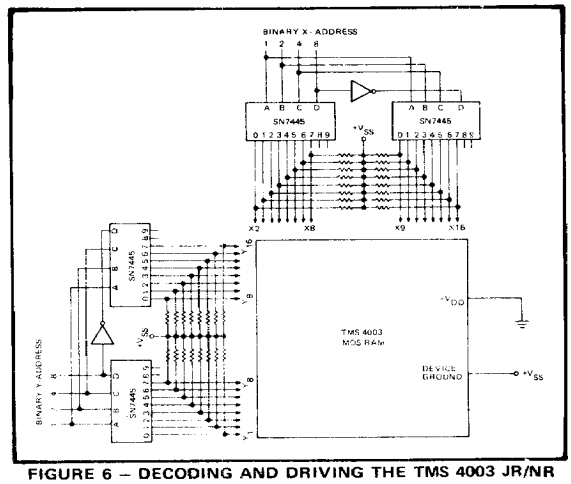


FIGURE 6 – DECODING AND DRIVING THE TMS 4003 JR/NR BY USE OF THE SN74154

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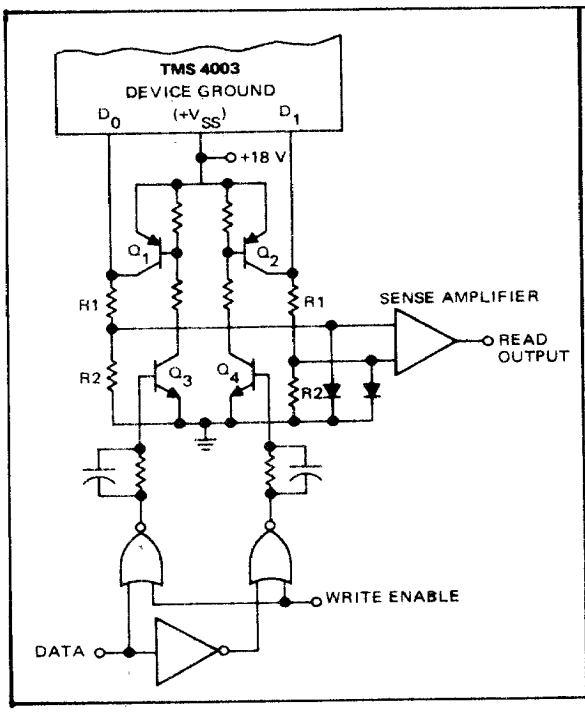
TYPICAL APPLICATION DATA (Continued)

TMS 4003 JR/NC MEMORIES WITH PARALLEL CONNECTED DIGIT LINES

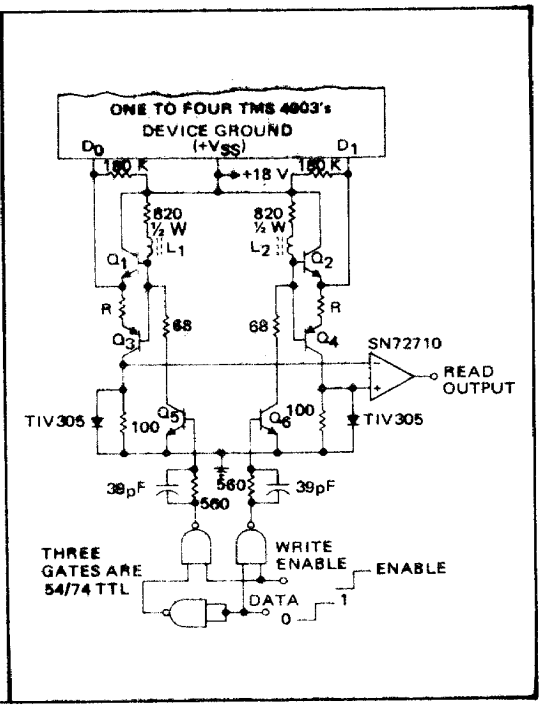


CIRCUIT COMPONENTS INFORMATION

Q1 and Q2: 2N3629
Q3 and Q4: 2N3014

FIGURE 7 -- BASIC READ/WRITE CIRCUIT LIMITED TO LOW-SPEED OPERATION

TMS 4003 JR/NC MEMORIES WITH PARALLEL CONNECTED DIGIT LINES



CIRCUIT COMPONENTS INFORMATION

L1 and L2: 2 1/2 T, No. 30 wire on Ferrite Bead (Allen-Bradley No. T0 135G144A or equivalent)
Q1, Q2, Q5, and Q6: 2N3014
Q3 and Q4: 2N3829

$$\text{R1 and R2: } \frac{180\ \Omega}{\text{No. of TMS 4003 JR memories}}$$

FIGURE 8 -- HIGH-SPEED READ/WRITE CIRCUIT

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