TMS 4023 NC
1024-BIT RANDOM-ACCESS MEMORY

features

- Low power dissipation
- Access time — 650 nsec (maximum)
- Cycle time — 900 ns (maximum
- Refresh Period — 2 ms for 0°C–70°C
- Fully decoded
- Wired-OR capability
- Inputs fully protected
- 24-lead plastic package

description

The TMS 4023 NC is a 1024-bit RAM, organized as 1024 one-bit words, using P-channel enhancement-mode transistors. A fully decoded monolithic array, the device is available in a low-cost, standard, 24-pin dual-in-line plastic package. The dynamic memory has nondestructive readout and refreshes all 1024 bits in 32 read cycles (or 32 microseconds). The TMS 4023 NC is designed as a low-cost main-frame memory for large-storage high-performance operations.

logic definition

Negative logic is assumed.

a) LOGICAL 1 = most negative voltage

b) LOGICAL 0 = most positive voltage

operation (refer to functional block diagram and timing diagram)

A 10-bit address code selects any one of the 1024 bits for either Read or Write operation. A Read or Write operation may be performed with the application of a logic 1 on the chip-enable line. The memory is inhibited with the application of a logic 0 to the chip-select line. This renders the data Input/Output line open and ineffective, which allows wired-OR operation. The address decode is not inhibited however.

Application of a logic 0 to the Read/Write line will result in a Read operation. This may be presented simultaneously with or before application of the address code. Read-out is nondestructive.

A logic 1 applied to the Read/Write and chip enable will result in a Write operation. Duration of the Write command must be at least 560 nanoseconds to ensure that the data is written into memory.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages V_{DD} and V_{SS} range (See Note 1)	−24 V to 0.3 V
Clock input voltage range (See Note 1)	−24 V to 0.3 V
Data input voltage range (See Note 1)	−24 V to 0.3 V
Operating free-air temperature range	−25°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SUB} (substrate).

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

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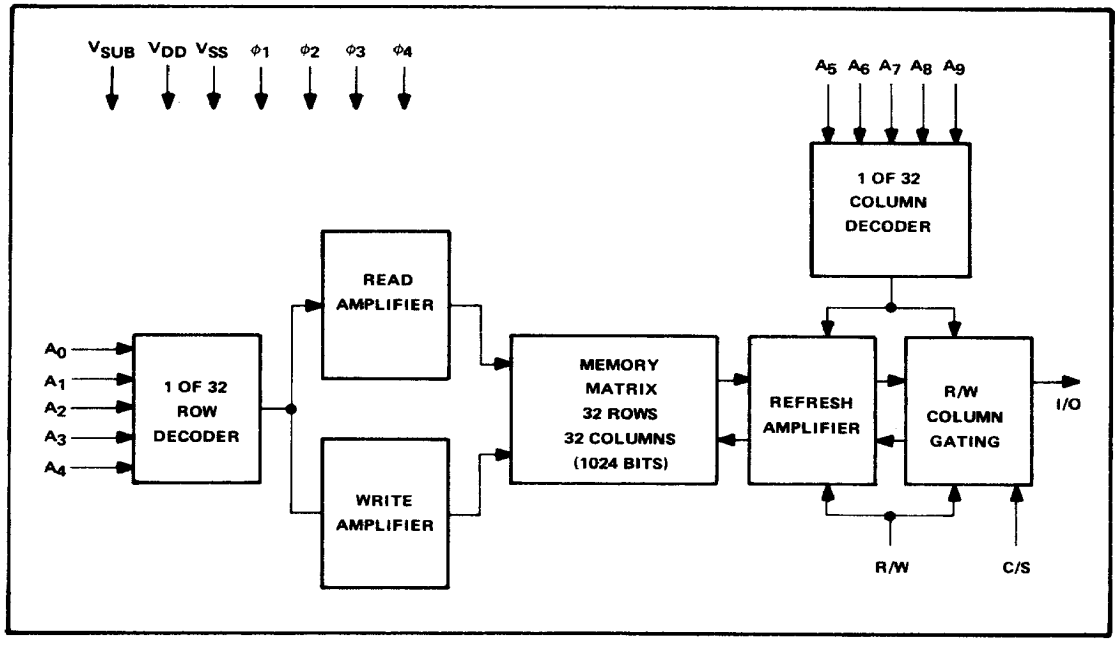
functional block diagram and pin configuration



recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage (See Note 1)				
Substrate Supply V_{SUB}	+1.5	+2.0	+2.5	V
V_{SS}		0		V
V_{DD}	−19	−20	−21	V
Logic Levels (See Note 1)				
Input HIGH level V_{IH}	−1.5		+0.3	V
Input LOW level V_{IL}	−19	−20	−21	V
Clock Voltage Levels (See Note 1)				
Clock HIGH level $V_{\phi H}$	−1.5		+0.3	V
Clock LOW level $V_{\phi L}$	−19	−20	−21	V
Pulse Timing				
Pulse widths				
Clock pulse width 1 $PW_{\phi 1}$	120			ns
Clock pulse width 2 $PW_{\phi 2}$	130			ns
Clock pulse width 3 $PW_{\phi 3}$	380			ns
Clock pulse width 4 $PW_{\phi 4}$	110			ns
Pulse Spacing				
Clock delay $t_{d\phi 1}$, $t_{d\phi 2}$, $t_{d\phi 3}$, $t_{d\phi 4}$	0			ns

NOTE 1: These voltage values are with respect to V_{SS}.

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recommended operating conditions (continued)

PARAMETER	MIN	NOM	MAX	UNITS
Pulse Spacing (continued)				
Address setup t_{AS}	10			ns
Address hold t_{AH}	10			ns
Chip-select setup time t_{CS}	0			ns
Chip-select hold time t_{CH}	0			ns
R/W overlap C/S t_{WS} and t_{WH}	10			ns
Data setup t_{DS}	10			ns
Data hold t_{DH}	10			ns
Refreshing time T_{REF}			2	ms

static electrical characteristics (under recommended operating conditions and for T_A = 0°C to 70°C)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Leakage Current					
Substrate				100	μA
Address Input				1	μA
Clock Input				1	μA
C/S Chip Select				1	μA
R/W Read/Write				1	μA
I/O Input/Output				1	μA
Output High Current					
I_{OS} Sense	R_{LOAD} = 200 Ω	1.1			mA
Supply Current Drain					
I_{DD} Drain Supply			1.0		mA

dynamic electrical characteristics (under recommended operating conditions and for T_A = 0°C to 70°C)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Cycle Time	C_{LOAD} = 100 pF,	900			ns
	R_{LOAD} = 200 Ω,				
t_{OD} Output Delay	V_{REF} = 180 mV			350	ns
t_{ACC} Access time (Note 2)	C_{LOAD} = 100 pF,		650		ns
	R_{LOAD} = 200 Ω,				
t_{AD} Available data on output	V_{REF} = 180 mV	50			ns
Capacitance					
C_{IN} Address Input			5	8	pF
$C_{\phi1}$, $C_{\phi2}$ Clock			17	20	pF
$C_{\phi3}$, $C_{\phi4}$			9	11	pF
C/S Chip Select			8	10	pF
R/W Read/Write					
I/O Input/Output					
Chip Selected			24	27	pF
Chip Not Selected			7	9	pF

NOTE 2: Access time is given for rise and fall times of input signals of no more than 15 ns.

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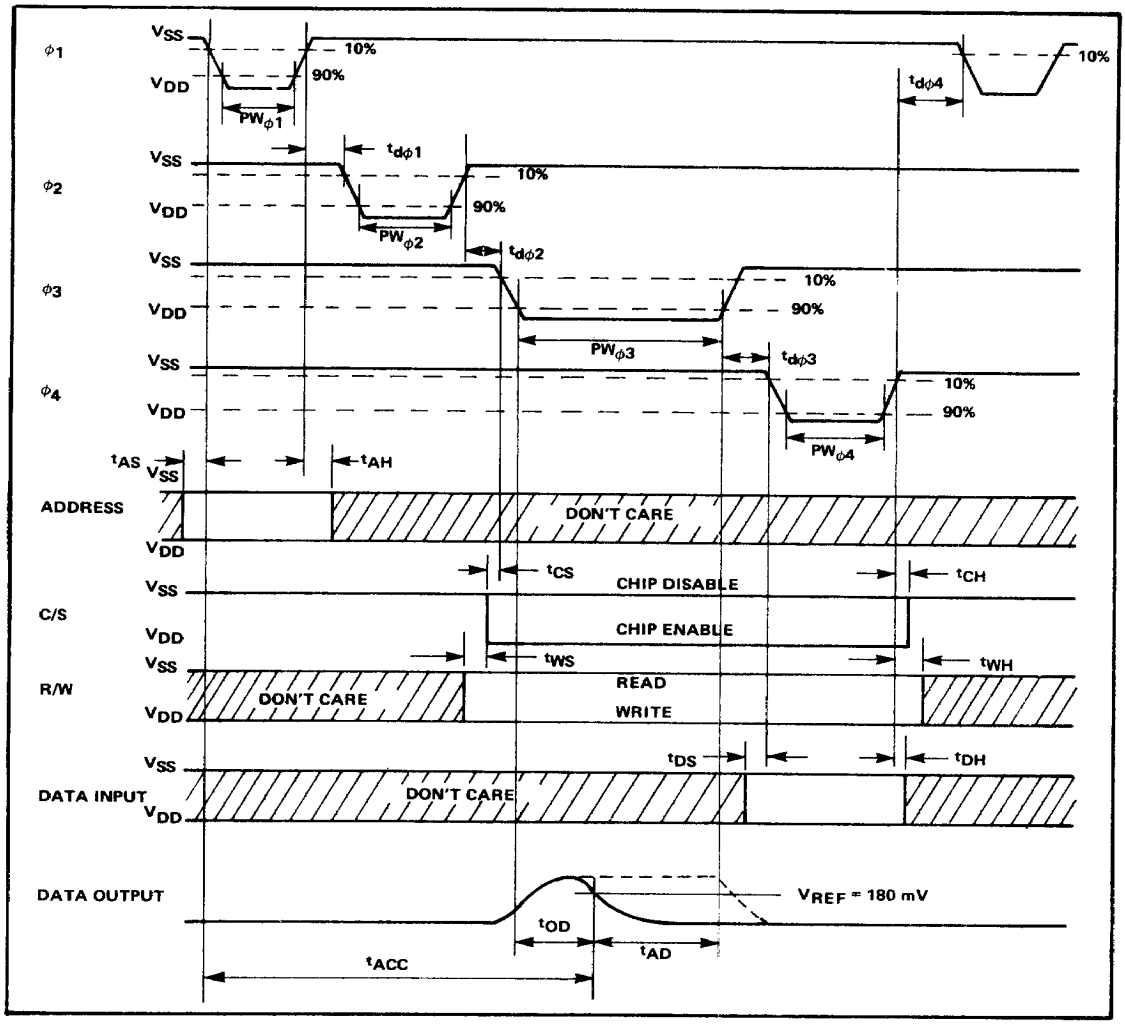
timing diagram and voltage waveforms



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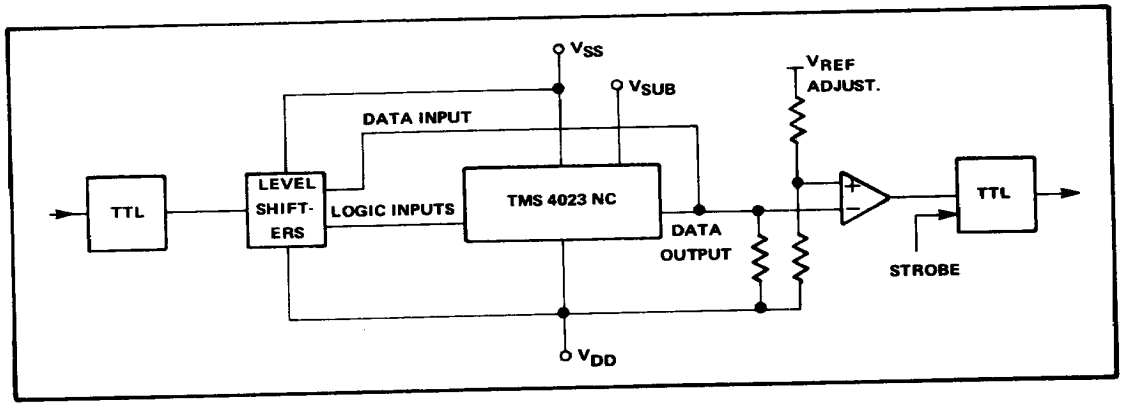
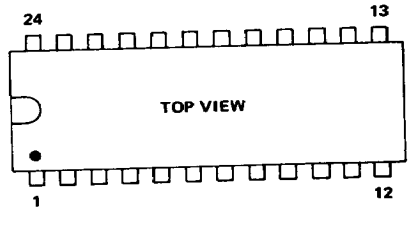
TTL interface



mechanical data and pin configuration

The TMS 4023 NC is mounted in a 24-pin dual-in-line plastic package, designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	–	13	–
2	A_9	14	I/O
3	A_8	15	C/S
4	A_7	16	R/W
5	V_{SS}	17	A_1
6	A_6	18	A_0
7	A_5	19	$\phi 3$
8	A_4	20	V_{DD}
9	A_3	21	$\phi 4$
10	A_2	22	$\phi 1$
11	–	23	$\phi 2$
12	–	24	V_{SUB}

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