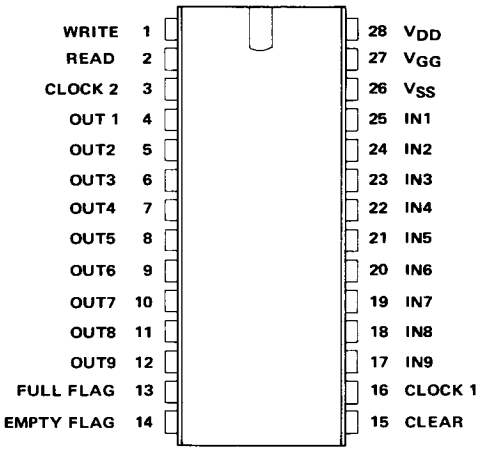
TMS 4024 JC, NC
9 X 64 DIGITAL STORAGE BUFFER (FIFO)

BULLETIN NO. DL-S 7512268, MAY 1975

- 64 Words of 9 Bits of Elastic Storage
- TTL-Compatibility on All Inputs Including Clocks
- 3-State Output Buffers
- 3 Control Inputs (Read, Write, Clear)
- DC to 250-kHz Data Rate
- Status Outputs (Full, Empty)
- Synchronous and Asynchronous Operation
- 2-Cycle (4-μs) Throughput
- Long-Term Data Retention
- Output Pins Directly Opposite Corresponding Inputs

28-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 4024 JC, NC is a first-in, first-out digital storage buffer that will store up to 64 nine-bit words. The major components of the device include a 9 x 64 dynamic RAM, three shift counters, and comparison and control logic. A RAM-type organization results in minimal ripple-through time. Data written at the input when the RAM is empty is available at the output two clock cycles later. The input and output are completely independent of each other. Input and output timing can be dependent on the clock timing (synchronous mode) or can be operated independently (asynchronous mode). The dynamic RAM requires two-phase continuous clocking at a specified minimum frequency. The clocks can be driven directly from TTL logic.

Low-threshold, thick-oxide, MOS p-channel enhancement-type technology is employed to allow interfacing with TTL circuits without external components.

The TMS 4024 is suitable for many applications as an interface between systems clocked at different speeds and in keyboard buffers, data concentrators, etc.

This device is offered in 28-pin dual-in-line ceramic (JC suffix) and plastic (NC suffix) packages designed for insertion in mounting-hole rows on 600-mil centers. The TMS 4024 is characterized for operation from $-25^{\circ}C$ to $85^{\circ}C$.

operation (refer to diagram "basic internal operation")

The TMS 4024 will process data at any desired rate from dc to one-half the continuous clock frequency with every other cycle used for automatic refresh. At a nominal 500-kHz clock rate the maximum data rate is 250 kHz. Data is processed in parallel format, word by word.

Writing and reading may be done either synchronously or asynchronously in relation to the clocks. Asynchronous operation is limited to data rates of less than one-third of the clock frequency. Read and write commands must have a minimum separation of one clock cycle.

A positive-going transition at the read or write input is recognized as a command and must occur a minimum time before the rise of clock 2.

A write command causes the data present at the input to be transferred into the buffer. Data-in must be valid for the period during which clock 2 is low. For asynchronous operation, data-in must be valid for two periods after a write command is given because a write command may be given at any time in relation to the clock.

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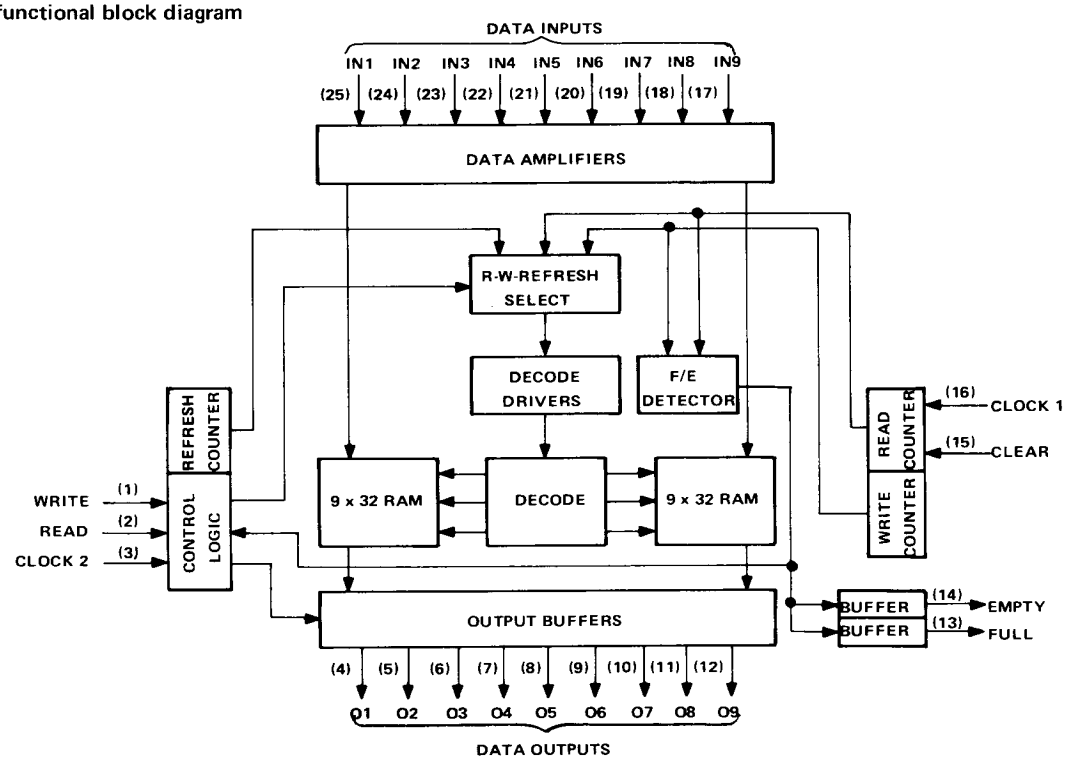
operation (continued)

If both read and write inputs are brought to a high logic level, the read and write operations are disabled and the data outputs float. The data present in the RAM is retained while the read and write operations are disabled.

A clear command will clear all contents of the digital storage buffer, except for the output latches. When the clear input is brought to a high level, it invalidates all other commands. Completion of a clear operation is detected by a high level at the empty status output. The clear command should be synchronized with clock 2.

Status outputs (empty and full) are provided to avoid invalid operation and to facilitate cascading of the device. A high level at the full status output invalidates write commands and a high level at the empty status output invalidates read commands.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	−15 V to 0.3 V
Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Clock input voltage range (see Note 1)	−15 V to 0.3 V
Data input voltage range (see Note 1)	−15 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings voltage values are with respect to V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to a floating ground.

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recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (see Note 2)	−4.75	−5	−5.25	V
Supply voltage, V_{GG} (see Note 2)	−10.8	−12	−13.2	V
Supply voltage, V_{SS} (see Note 2)	4.75	5	5.25	V
High-level input voltage, all inputs including clocks, V_{IH} (see Note 3)	V_{SS} −1.5	3.5	V_{SS}	V
Low-level input voltage, all inputs including clocks, V_{IL} (see Note 3)	−5.5	0	0.3	V
Clock pulse rise time, $t_{r(\phi)}$		25	50	ns
Clock pulse fall time, $t_{f(\phi)}$		25	50	ns
Clock-1 pulse width, $t_{w(\phi1)}$	400	700		ns
Clock-2 pulse width, $t_{w(\phi2)}$	700	1000		ns
Read pulse width, $t_{w(rd)}$	300	2000		ns
Write pulse width, $t_{w(wr)}$	300	2000		ns
Clear pulse width, $t_{w(clr)}$	1			ck cyc
Delay time, clock 1 to clock 2, $t_{d(\phi1\text{-}\phi2)}$	300			ns
Delay time, clock 2 to clock 1, $t_{d(\phi2\text{-}\phi1)}$	0	300		ns
Delay time, clock 2 to clock 1, plus clock-1 pulse width, $t_{d(\phi2\text{-}\phi1)} + t_{w(\phi1)}$	1000			ns
Delay time, read to clock 2, $t_{d(rd\text{-}\phi2)}$	400	600		ns
Delay time, write to clock 2, $t_{d(wr\text{-}\phi2)}$	400	600		ns
Data setup time, $t_{su(da)}$	350			ns
Data hold time, $t_{h(da)}$		350		ns
Data input frequency, f_{data}	0		250	kHz
Clock frequency, f_{ϕ}	120		500	kHz
Operating free-air temperature, T_A	−25		85	°C

NOTES:
2. Voltage values are with respect to a floating ground.
3. The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.
4. Nominal timing is given for 500-kHz operation.

electrical characteristics under nominal operating conditions, T_A = −25°C to 85°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −0.5 mA	V_{SS} −1	V_{SS} −0.5	V_{SS}	V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA (see Note 5)		0	0.4	V
I_I	Input current, all inputs including clocks				1000	nA
$I_{DD(avg)}$	Average supply current from V_{DD} (see Note 6)	MOS load		−8		mA
$I_{GG(avg)}$	Average supply current from V_{GG} (see Note 6)	MOS load		−6		mA
P_D	Power dissipation	MOS load		182		mW
C_i	Input capacitance, all inputs including clock	f = 100 kHz		7		pF

†All typical values are at T_A = 25°C.

NOTES:
5. V_{OL} is measured with a 1.5-kΩ resistor in series with the output and includes the drop across the resistor.
6. Typical values of $I_{DD(avg)}$ and $I_{GG(avg)}$ are −25 mA and −8 mA at 85°C, each output driving a Series 74 TTL load with a 1.5-kΩ resistor in series, a 25% clock duty cycle (% of time clock is high) and a 75% output current duty cycle (% of time outputs are low).
Typical values of $I_{DD(avg)}$ and $I_{GG(avg)}$ are −60 mA and −8 mA at 85°C, each output driving a Series 74 TTL load with no resistor in series, a 25% clock duty cycle and all outputs low continuously.

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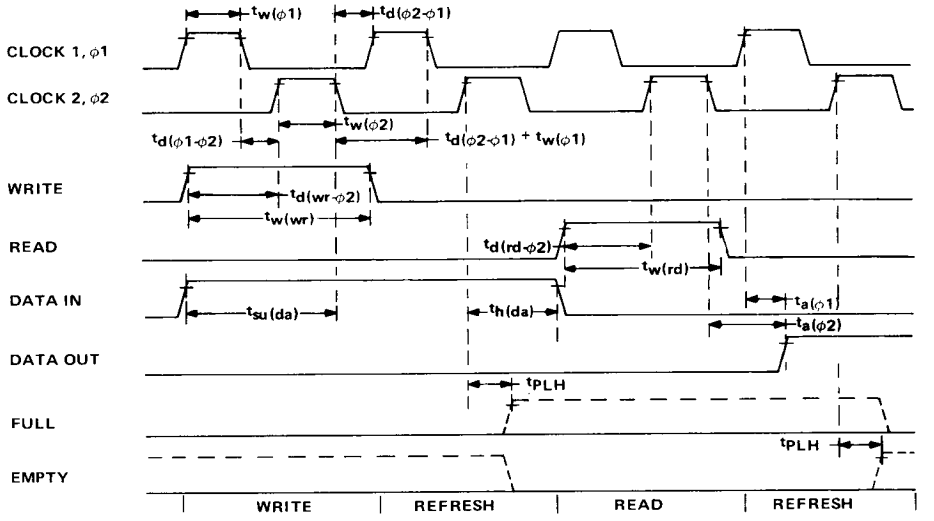
switching characteristics under nominal operating conditions, T_A = −25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{a(\phi1)}$	Access time from clock 1	1 Series 74 TTL load, 25 pF in parallel, 1.5 kΩ in series		400		ns
$t_{a(\phi2)}$	Access time from clock 2		950	1000	1200	ns
t_{PLH}	Propagation delay time, low-to-high level flag outputs from clock 2			400		ns

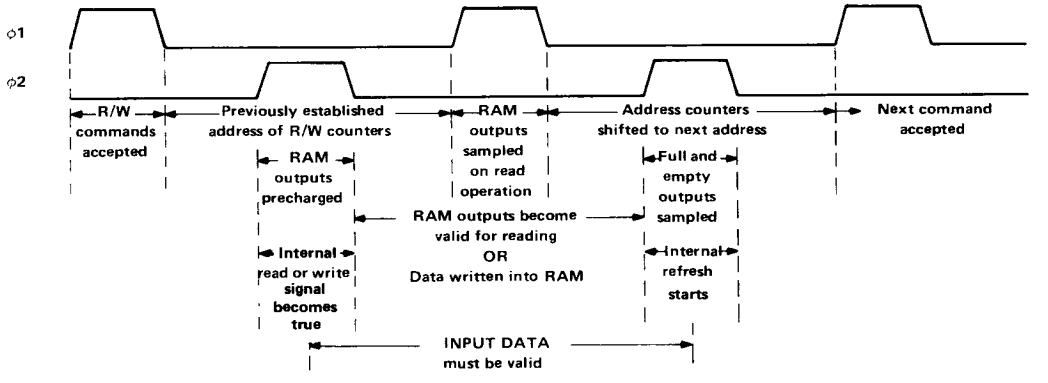
†All typical values are at T_A = 25°C.

timing diagram and voltage waveforms



NOTE: Timing points are 90% (high) and 10% (low).

basic internal operation



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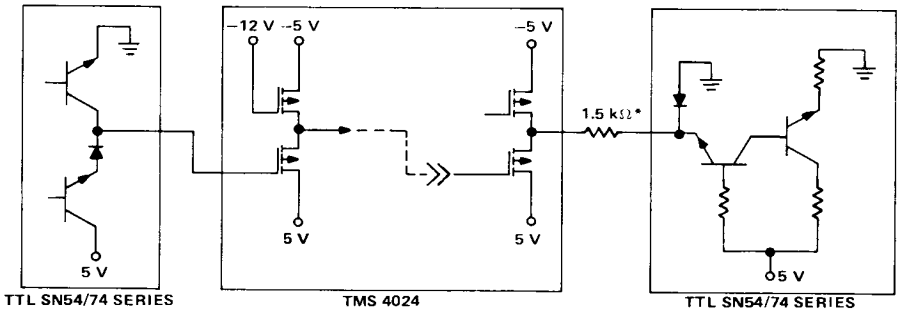
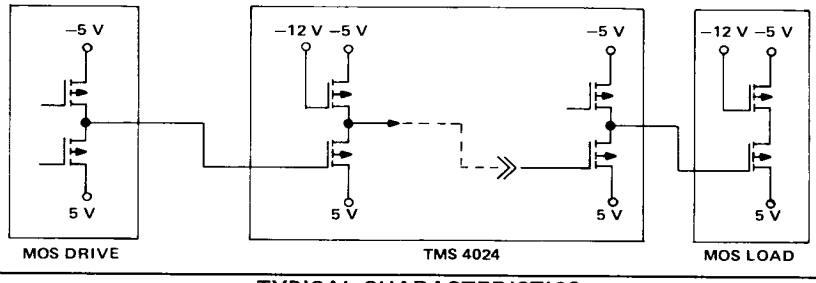
interface circuits

a) TTL



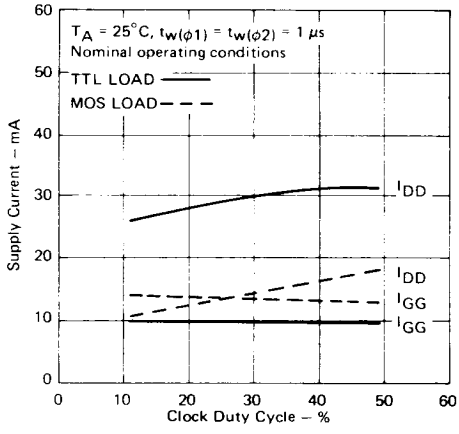
*1.5 kΩ resistor optional – the presence of this resistor helps to reduce power dissipation in the TMS 4024 while driving TTL.

b) MOS

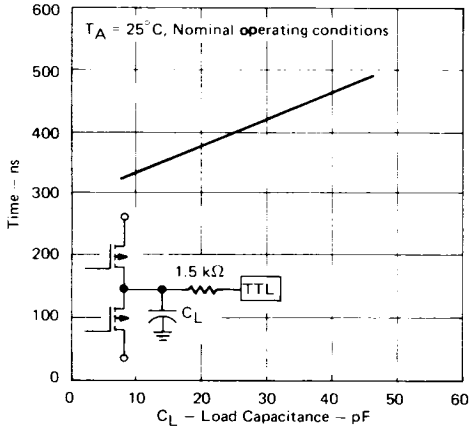


TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs DUTY CYCLE



PROPAGATION DELAY TIMES FOR FULL OR EMPTY FLAGS FROM CLOCK 2 OR ACCESS TIME FROM CLOCK 1 vs LOAD CAPACITANCE



NOTE: TTL load, 1.5 kΩ series resistor, all outputs low; MOS load, all outputs high.

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