



8228/8238 SYSTEM CONTROLLER AND BUS DRIVER FOR 8080A CPU

- Single Chip System Control for MCS[®]-80 Systems
- Built-In Bidirectional Bus Driver for Data Bus Isolation
- Allows the Use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge
- Reduces System Package Count
- User Selected Single Level Interrupt Vector (RST 7)
- 8238 Has Advanced IOW/MEMW for Large System Timing Control
- Available in EXPRESS — Standard Temperature Range
- Available in 28-Lead Cerdip and Plastic Packages

(See Packaging Spec, Order #231369)

The Intel[®] 8228 is a single chip system controller and bus driver for MCS[®]-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bidirectional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems designer to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The 8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an interrupt acknowledge by the 8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The 8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable design of MCS-80 systems.

NOTE:

The specifications for the 3228/3238 are identical with those for the 8228/8238.

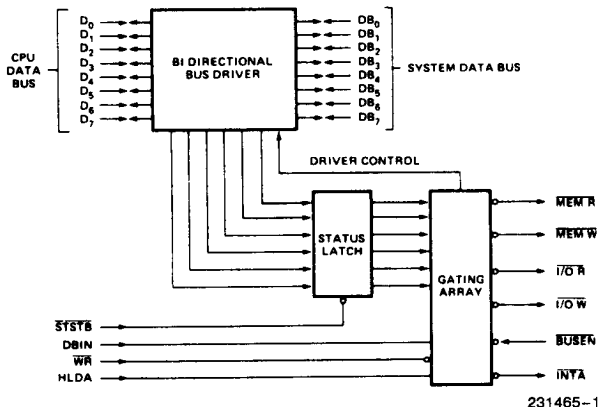
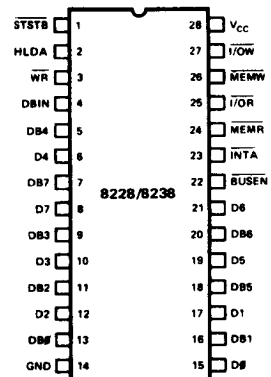


Figure 1. Block Diagram

231465-1



231465-2

D7-DO	Data Bus (8080 Side)	INTA	Interrupt Acknowledge
DB7-DB0	Data Bus (System Side)	HLDA	HLDA (from 8080)
I/O R	I/O Read	WR	WR (from 8080)
I/O W	I/O Write	BUSEN	Bus Enable Input
MEMR	Memory Read	STSTB	Status Strobe (from 8224)
MEMW	Memory Write	VCC	+5V
DBIN	DBIN (from 8080)	GND	0 Volts

Figure 2. Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-0°C to 70°C
Storage Temperature	-65°C to +150°C
Supply Voltage, V_{CC}	-0.5V to +7V
Input Voltage	-1.5 to +7V
Output Current	100 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ(1)	Max		
V_C	Input Clamp Voltage, All Input			0.75	-1.0	V	$V_{CC} = 4.75\text{V}$; $I_C = -5\text{ mA}$
I_F	Input Load Current	STSTB			500	μA	$V_{CC} = 5.25\text{V}$
		D_2 & D_6			750	μA	$V_F = 0.45\text{V}$
		$D_0, D_1, D_4,$ D_5 & D_7			250	μA	
		All Other Inputs			250	μA	
I_R	Input Leakage Current	STSTB			100	μA	$V_{CC} = 5.25\text{V}$ $V_R = 5.25\text{V}$
		DB_0 - DB_7			20	μA	
		All Other Inputs			100	μA	
V_{TH}	Input Threshold Voltage, All Inputs		0.8		2.0	V	$V_{CC} = 5\text{V}$
I_{CC}	Power Supply Current			140	190	mA	$V_{CC} = 5.25\text{V}$
V_{OL}	Output Low Voltage	D_0 - D_7			0.45	V	$V_{CC} = 4.75\text{V}$; $I_{OL} = 2\text{ mA}$
		All Other Outputs			0.45	V	$I_{OL} = 10\text{ mA}$
V_{OH}	Output High Voltage	D_0 - D_7	3.6	3.8		V	$V_{CC} = 4.75\text{V}$; $I_{OH} = -10\mu\text{A}$
		All Other Outputs	2.4			V	$I_{OH} = -1\text{ mA}$
I_{OS}	Short Circuit Current, All Outputs		15		90	mA	$V_{CC} = 5\text{V}$
$I_{O(off)}$	Off State Output Current All Control Outputs				100	μA	$V_{CC} = 5.25\text{V}$; $V_O = 5.25\text{V}$
					-100	μA	$V_O = 0.45\text{V}$
I_{INT}	INTA Current				5	mA	(See INTA Test Circuit)

NOTE:

1. Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltages.

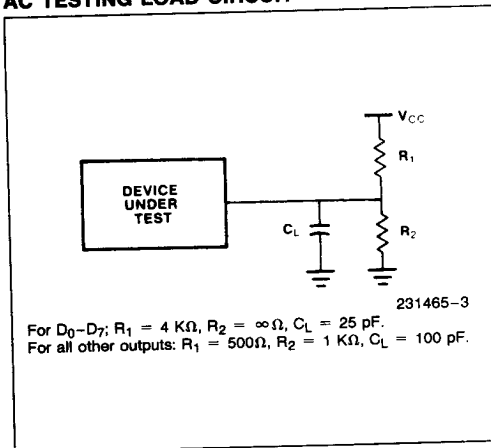
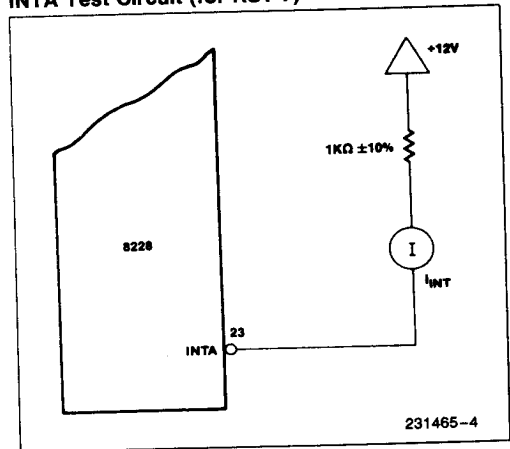
CAPACITANCE $V_{BIAS} = 2.5V, V_{CC} = 5.0V, T_A = 25^\circ C, f = 1 \text{ MHz}$

1. This parameter is periodically sampled and not 100% tested.

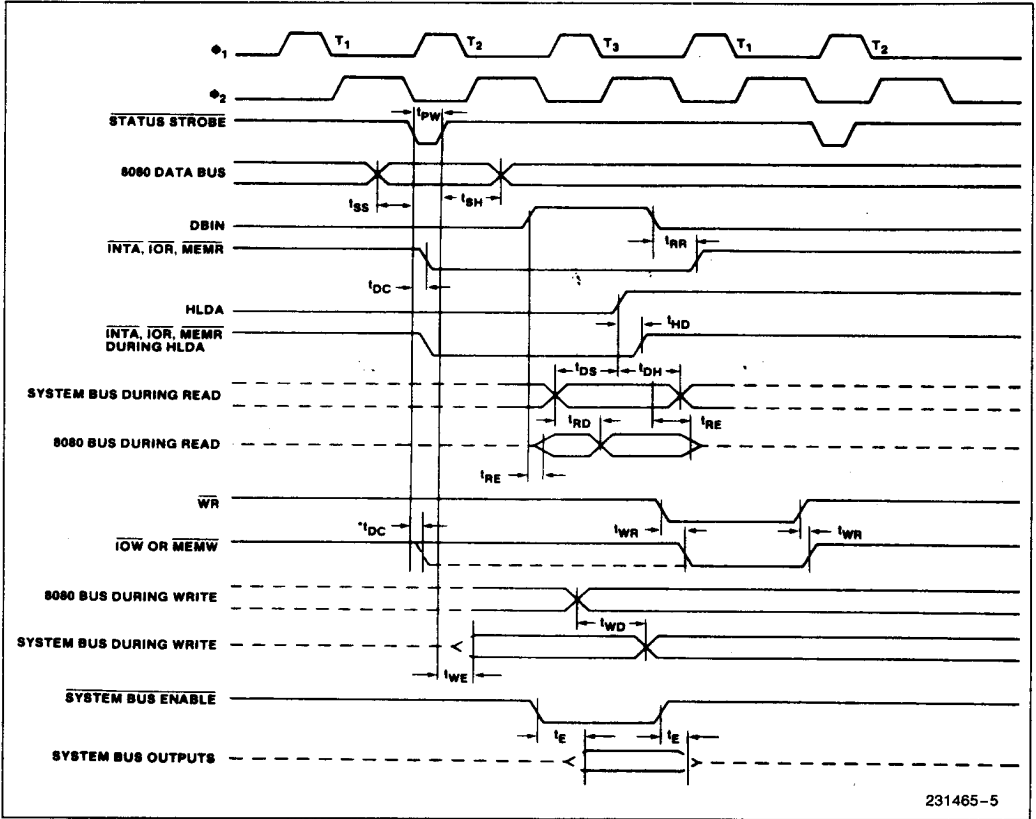
Symbol	Parameter	Limits			Unit
		Min	Typ(1)	Max	
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

A.C. CHARACTERISTICS $T_A = 0^\circ C \text{ to } 70^\circ C, V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Limits		Unit	Conditions
		Min	Max		
t_{PW}	Width of Status Strobe		22	ns	
t_{SS}	Setup Time, Status Inputs D_0-D_7	8		ns	
t_{SH}	Hold Time, Status Inputs D_0-D_7	5		ns	
t_{DC}	Delay from \overline{STSTB} to any Control Signal	20	60	ns	$C_L = 100 \text{ pF}$
t_{RR}	Delay from \overline{DBIN} to Control Outputs		30	ns	$C_L = 100 \text{ pF}$
t_{RE}	Delay from \overline{DBIN} to Enable/Disable 8080 Bus		45	ns	$C_L = 25 \text{ pF}$
t_{RD}	Delay from System Bus to 8080 Bus during Read		30	ns	$C_L = 25 \text{ pF}$
t_{WR}	Delay from \overline{WR} to Control Outputs	5	45	ns	$C_L = 100 \text{ pF}$
t_{WE}	Delay to Enable System Bus DB_0-DB_7 after \overline{STSTB}		30	ns	$C_L = 100 \text{ pF}$
t_{WD}	Delay from 8080 Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	5	40	ns	$C_L = 100 \text{ pF}$
t_E	Delay from System Bus Enable to System Bus DB_0-DB_7		30	ns	$C_L = 100 \text{ pF}$
t_{HD}	HLDA to Read Status Outputs		25	ns	
t_{DS}	Setup Time, System Bus Inputs to HLDA	10		ns	
t_{DH}	Hold Time, System Bus Inputs to HLDA	20		ns	$C_L = 100 \text{ pF}$

AC TESTING LOAD CIRCUIT

INTA Test Circuit (for RST 7)


WAVEFORMS



231465-5

VOLTAGE MEASUREMENT POINTS: D₀-D₇ (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

NOTE:
*ADVANCED IOW/MEMW for 8238 ONLY.