

Handwritten notes:
 4096 words x 1 bit
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4096 BIT DYNAMIC RAMS

DESCRIPTION The μPD411A Family consists of four 4096 words by 1 bit dynamic N-channel MOS RAMs. They are designed for memory applications where very low cost and large bit storage are important design objectives. The μPD411A Family is designed using dynamic circuitry which reduces the standby power dissipation.

Reading information from the memory is non-destructive. Refreshing is easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic high or a logic low.

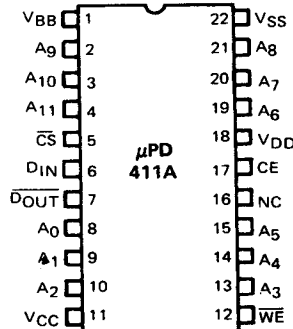
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FEATURES

- Low Standby Power
- 4096 words x 1 bit Organization
- A single low-capacitance high level clock input with solid ±1 volt margins.
- Inactive Power 0.7 mW (Typ.)
- Power Supply +12, +5, -5V
- Easy System Interface
- TTL Compatible (Except CE)
- Address Registers on the Chip
- Simple Memory Expansion by Chip Select
- Three State Output and TTL Compatible
- 22 pin Plastic Dual-in-Line Package
- Replacement for INTEL's 2107B, TI's 4060 and Equivalent Devices.
- 3 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE	REFRESH TIME
μPD411A	300 ns	470 ns	650 ns	2 ms
μPD411A-1	250 ns	430 ns	600 ns	2 ms
μPD411A-2	200 ns	400 ns	520 ns	2 ms

PIN CONFIGURATION



PIN NAMES

A0 - A11	Address Inputs
A0 - A5	Refresh Addresses
CE	Chip Enable
CS	Chip Select
DIN	Data Input
DOUT	Data Output
WE	Write Enable
VDD	Power (+12V)
VCC	Power (+5V)
VSS	Ground
VBB	(Power, -5V)
NC	No Connection

Rev/1

μPD411A

CE Chip Enable

A single external clock input is required. All read, write, refresh and read-modify-write operations take place when chip enable input is high. When the chip enable is low, the memory is in the low power standby mode. No read/write operations can take place because the chip is automatically precharging.

$\overline{\text{CS}}$ Chip Select

The chip select terminal affects the data in, data out and read/write inputs. The data input and data output terminals are enabled when chip select is low. The chip select input must be low on or before the rising edge of the chip enable and can be driven from standard TTL circuits. A register for the chip select input is provided on the chip to reduce overhead and simplify system design.

$\overline{\text{WE}}$ Write Enable

The read or write mode is selected through the write enable input. A logic high on the $\overline{\text{WE}}$ input selects the read mode and a logic low selects the write mode. The $\overline{\text{WE}}$ terminal can be driven from standard TTL circuits. The data input is disabled when the read mode is selected.

A₀–A₁₁ Addresses

All addresses must be stable on or before the rising edge of the chip enable pulse. All address inputs can be driven from standard TTL circuits. Address registers are provided on the chip to reduce overhead and simplify system design.

D_{IN} Data Input

Data is written during a write or read-modify-write cycle while the chip enable is high. The data in terminal can be driven from standard TTL circuits. There is no register on the data in terminal.

D_{OUT} Data Output

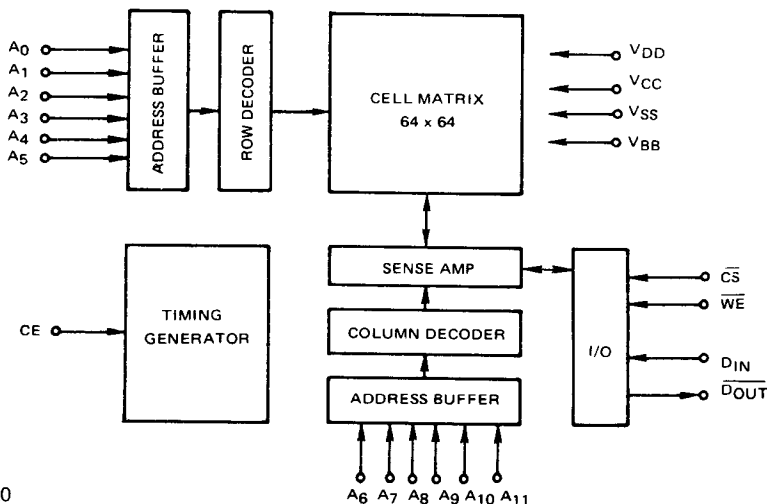
The three state output buffer provides direct TTL compatibility with a fan-out of two TTL gates. The output is in the high-impedance (floating) state when the chip enable is low or when the Chip Select input is high. Data output is inverted from data in.

Refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs A₀ through A₅ or by addressing every row within any 2-millisecond period. Addressing any row refreshes all 64 bits in that row.

The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, the chip select must be high.

FUNCTIONAL DESCRIPTION



BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to +125°C
Output Voltage ①	+20 to -0.3 Volts
All Input Voltages ①	+20 to -0.3 Volts
Supply Voltage V _{DD} ①	+20 to -0.3 Volts
Supply Voltage V _{CC} ①	+20 to -0.3 Volts
Supply Voltage V _{SS} ①	+20 to -0.3 Volts
Power Dissipation	1.0W

Note: ① Relative to V_{BB}.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. ①	MAX.		
Input Load Current	I _{LI}		0.01	10	μA	V _{IN} = V _{IL} MIN to V _{IH} MAX
CE Input Load Current	I _{LC}		0.01	10	μA	V _{IN} = V _{ILC} MIN to V _{IHC} MAX
Output Leakage Current for High Impedance State	I _{LO}		0.01	±10	μA	CE = V _{ILC} or \overline{CS} = V _{IH} V _O = 0V to 5.25V
V _{DD} Supply Current during CE off	I _{DD OFF}		50	200	μA	CE = -1.0V to 0.6V
V _{DD} Supply Current during CE on	I _{DD ON}		35	50	mA	CE = V _{IHC} , T _a = 25°C
Average V _{DD} Current μPD411A μPD411A-1 μPD411A-2	I _{DD AV} I _{DD AV} I _{DD AV}		38 38 38	55 55 55	mA mA mA	T _a = 25°C Cycle Time = 470 ns Cycle Time = 430 ns Cycle Time = 400 ns
V _{BB} Supply Current ②	I _{BB}		5	100	μA	
V _{CC} Supply Current during CE off ③	I _{CC OFF}		0.01	10	μA	CE = V _{ILC} or \overline{CS} = V _{IH}
Input Low Voltage	V _{IL}	-1.0		0.6	V	
Input High Voltage	V _{IH}	2.4		V _{CC} + 1	V	
CE Input Low Voltage	V _{ILC}	-1.0		0.6	V	
CE Input High Voltage	V _{IHC}	V _{DD} - 1	V _{DD}	V _{DD} + 1	V	
Output Low Voltage	V _{OL}	0		0.40	V	I _{OL} = 3.2 mA
Output High Voltage	V _{OH}	2.4		V _{CC}	V	I _{OH} = -2.0 mA

- Notes: ① Typical values are for T_a = 25°C and nominal power supply voltages.
 ② The I_{BB} current is the sum of all leakage currents.
 ③ During CE on V_{CC} supply current is dependent on output loading.

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Address Capacitance	C _{AD}			6	pF	V _{IN} = V _{SS}
\overline{CS} Capacitance	C _{CS}			6	pF	V _{IN} = V _{SS}
D _{IN} Capacitance	C _{IN}			6	pF	V _{IN} = V _{SS}
\overline{DOUT} Capacitance	C _{OUT}			7	pF	V _{OUT} = V _{SS}
\overline{WE} Capacitance	C _{WE}			7	pF	V _{IN} = V _{SS}
CE Capacitance	CCE1			27	pF	V _{IN} = V _{SS}
	CCE2			22	pF	V _{IN} = V _{DD}

READ CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		μPD411A		μPD411A-1		μPD411A-2			
		MIN	MAX	MIN	MAX	MIN	MAX		
Time Between Refresh	tREF		2		2		2	ms	tT = tr = tf = 20 ns CL = 50 pF Load = 1TTL Gate Vref = 2.0 or 0.8 Volts
Address to CE Set Up Time	tAC	0		0		0		ns	
Address Hold Time	tAH	150		150		150		ns	
CE Off Time	tCC	130		130		130		ns	
CE Transition Time	tT	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	tCF	0	130	0	130	0	130	ns	
Cycle Time	tCY	470		430		400		ns	
CE on Time	tCE	300	3000	260	3000	230	3000	ns	
CE Output Delay	tCO		280		230		180	ns	
Access Time	tACC		300		250		200	ns	
CE to WE	tWL	40		40		40		ns	
WE to CE on	tWC	0		0		0		ns	

WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		μPD411A		μPD411A-1		μPD411A-2			
		MIN	MAX	MIN	MAX	MIN	MAX		
Cycle Time	tCY	470		430		400		ns	tT = tr = tf = 20 ns CL = 50 pF Load = 1TTL Gate Vref = 2.0 or 0.8 Volts
Time Between Refresh	tREF		2		2		2	ms	
Address to CE Set Up Time	tAC	0		0		0		ns	
Address Hold Time	tAH	150		150		150		ns	
CE Off Time	tCC	130		130		130		ns	
CE Transition Time	tT	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	tCF	0	130	0	130	0	130	ns	
CE on Time	tCE	300	3000	260	3000	230	3000	ns	
WE to CE off	tW	180		180		150		ns	
CE to WE	tCW	300		260		230		ns	
DIN to WE Set Up ^①	tDW	0		0		0		ns	
DIN Hold Time	tDH	40		40		40		ns	
WE Pulse Width	tWP	180		180		150		ns	

Note ① If WE is low before CE goes high then DIN must be valid when CE goes high.

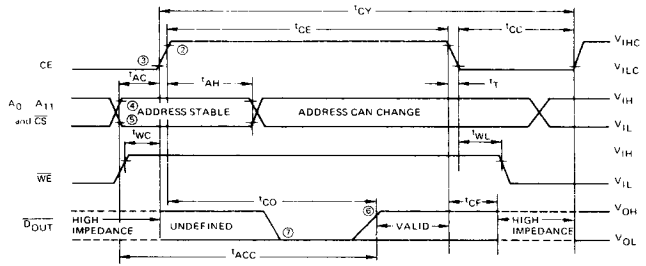
READ-MODIFY-WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

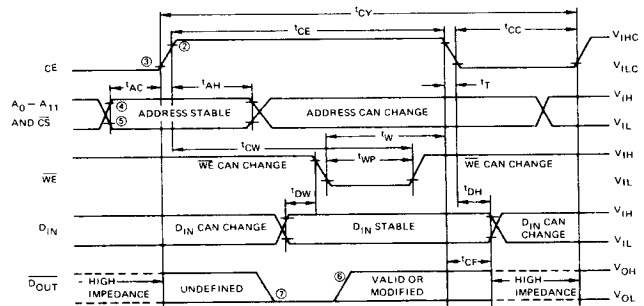
PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		μPD411A		μPD411A-1		μPD411A-2			
		MIN	MAX	MIN	MAX	MIN	MAX		
Read-Modify-Write (RMW) Cycle Time	tRWC	650		600		520		ns	tT = tr = tf = 20 ns CL = 50 pF Load = 1TTL Gate Vref = 2.0 or 0.8 Volts
Time Between Refresh	tREF		2		2		2	ms	
Address to CE Set Up Time	tAC	0		0		0		ns	
Address Hold Time	tAH	150		150		150		ns	
CE Off Time	tCC	130		130		130		ns	
CE Transition Time	tT	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	tCF	0	130	0	130	0	130	ns	
CE Width During RMW	tCRW	480	3000	430	3000	350	3000	ns	
WE to CE on	tWC	0		0		0		ns	
WE to CE off	tW	180		180		150		ns	
WE Pulse Width	tWP	180		180		150		ns	
DIN to WE Set Up	tDW	0		0		0		ns	
DIN Hold Time	tDH	40		40		40		ns	
CE to Output Delay	tCO		280		230		180	ns	
Access Time	tACC		300		250		200	ns	

TIMING WAVEFORMS

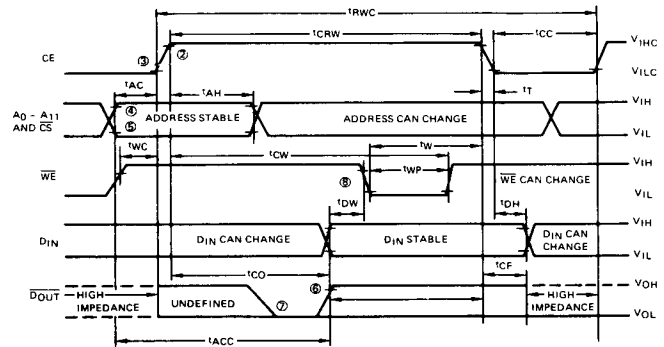
READ AND REFRESH CYCLE ①



WRITE CYCLE



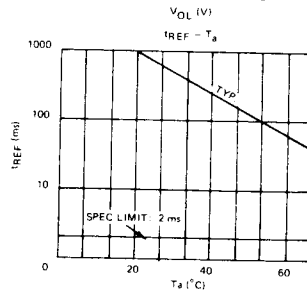
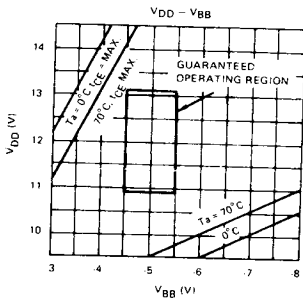
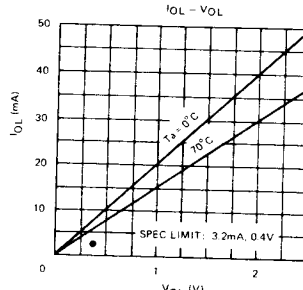
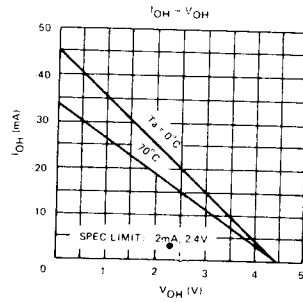
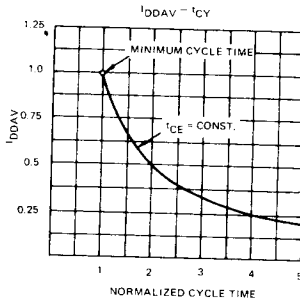
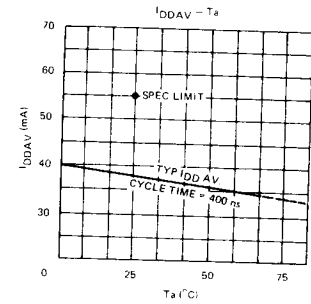
READ-MODIFY-WRITE CYCLE



- Notes:
- ① For refresh cycle, row and column addresses must be stable t_{AC} and remain stable for entire t_{AH} period.
 - ② $V_{DD} - 2V$ is the reference level for measuring timing of CE.
 - ③ $V_{SS} + 2V$ is the reference level for measuring timing of CE.
 - ④ V_{IHMIN} is the reference level for measuring timing of the addresses, CS, WE and DIN.
 - ⑤ V_{ILMAX} is the reference level for measuring timing of the addresses, CS, WE and DIN.
 - ⑥ $V_{SS} + 2.0V$ is the reference level for measuring timing of \overline{DOUT} .
 - ⑦ $V_{SS} + 0.8V$ is the reference level for measuring timing of \overline{DOUT} .
 - ⑧ WE must be at V_{IH} until end of t_{CO} .

μPD411A

TYPICAL OPERATING CHARACTERISTICS



Power consumption = $V_{DD} \times I_{DDAV} + V_{BB} \times I_{BB}$

POWER CONSUMPTION

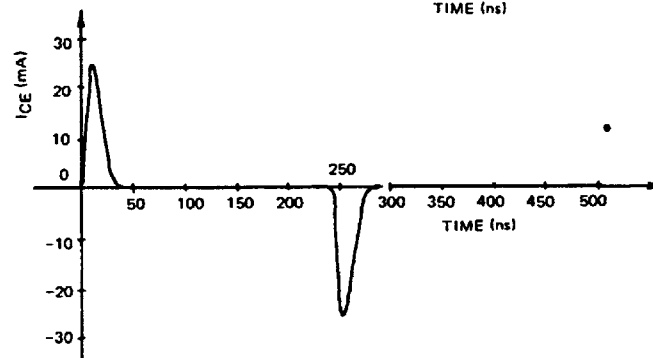
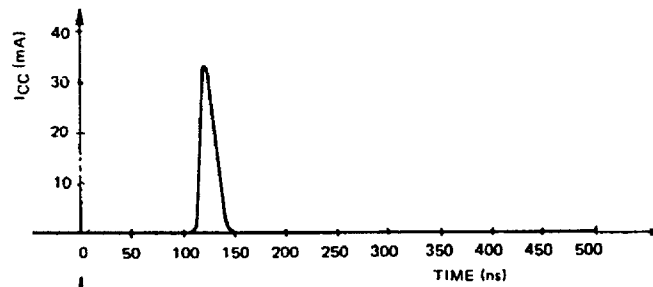
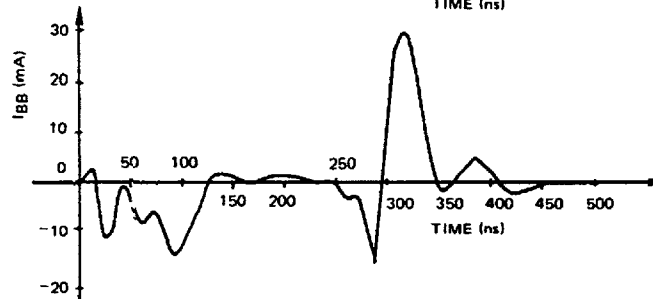
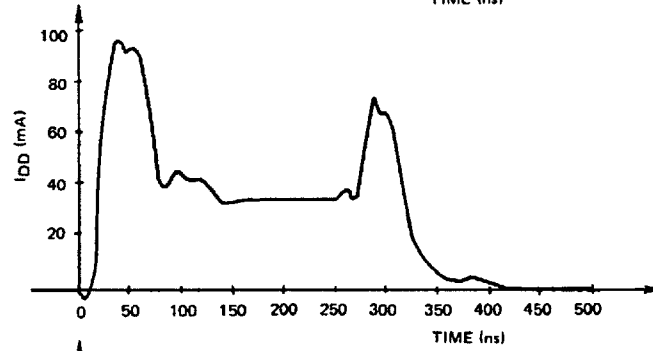
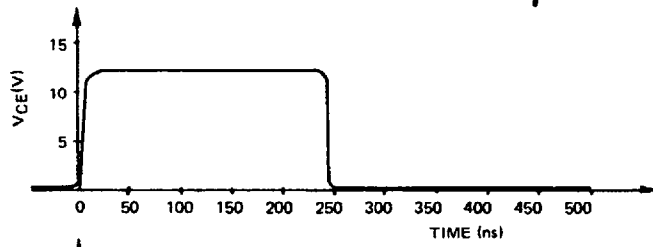
Typical power dissipation for each product is shown below.

	mW (TYP.)	CONDITIONS
μPD411A	460 mW	$T_a = 25^\circ\text{C}$, $t_{cy} = 470 \text{ ns}$, $t_{CE} = 300 \text{ ns}$
μPD411A-1	460 mW	$T_a = 25^\circ\text{C}$, $t_{cy} = 430 \text{ ns}$, $t_{CE} = 260 \text{ ns}$
μPD411A-2	460 mW	$T_a = 25^\circ\text{C}$, $t_{cy} = 400 \text{ ns}$, $t_{CE} = 230 \text{ ns}$

See curve above for power dissipation versus cycle time.

CURRENT WAVEFORMS ①

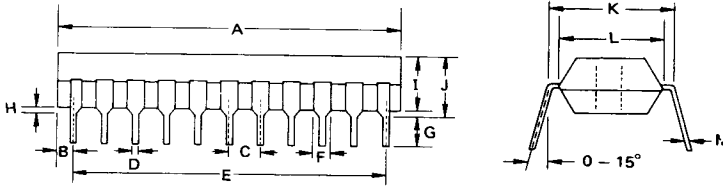
μPD411A



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μ PD411A

**PACKAGE OUTLINE
μPD411AC**



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50	0.02
E	25.4	1.00
F	1.40	0.055
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	0.25 ^{+0.10} _{-0.05}	0.01 ^{+0.004} _{-0.002}